MXCHIP®

Datasheet

EMC3380 Wi-Fi/BT Module

Built-in ARM Cortex V8 dual-core processor, voice processor and Flash memory.

2.4/5G Hz dual-frequency Wi-Fi, BLE 5.0, audio processing unit, PSRAM, rich peripherals

Version：3.4 Date：2020-04-27 Number：DS0144EN

Abstract

- **Input voltage：3.0V~3.3V**
- **Processor：Dual-core CPU with ARM v8-M architecture.**
  - Performance core KM4：Cortex-M33 with main frequency up to 200MHz.
  - Energy Efficiency Core KM0：Cortex-M23 with main frequency up to 20MHz.
  - Deep Sleep、Deep Standby and Sleep mode.
  - SWD/JTAG simulation debugging interface.
- **Memory**
  - 512K bytes SRAM for KM4 core
  - 64K bytes SRAM for KM0 core
  - 4M bytes PSRAM
  - XIP flash memory from 2M to 16M bytes
- **Wi-Fi**
  - 802.11 a/b/g/n 1T1R 2.4/5GHz dual frequency.
  - Processing Wi-Fi messages using independent Microcontrollers.
  - Support low power TX/RX mode in short distance applications.
  - Support narrow-band mode: 10MHz bandwidth.
  - Support Antenna diversity.
  - Support the IEEE Power Save Model
- **BT 5.0 Low Energy**
  - Comply with Low Power Bluetooth 5.0 Standard.
  - Support high power mode (10dbm).
  - Wi-Fi and BLE time division multiplexing and share the same PA and antenna.
  - Support Bluetooth Master-Slave Mode and BLE mesh.
- **Audio Codec**
  - Support 8, 16, 32, 44.1, 48 and 96 kHz sampling rates
  - 24-bit stereo DAC and DAC
  - Headphone speakers supporting 16ohm and 32ohm loads
  - Two Digital Microphone Interfaces
  - Bias Voltage of Built-in Microphone
  - Optional Voice Processor for Intelligent Noise Reduction
- **I2S Interface**

- Output: 16/24 bit，24K-384K Sampling rate stereo.
- Input: 16 bit，24K-96K Sampling rate dual microphone.
- Full duplex input/output stereo audio
- 5.1 Channel Output.

- **Safety**
  - ARM Trust Zone-M Technology.
  - AES/SHA Hardware Accelerator, Random Number Generator
  - Security boot Safe Start
  - Anti-reading mechanism: JTAG interface protection, flash encryption technology.

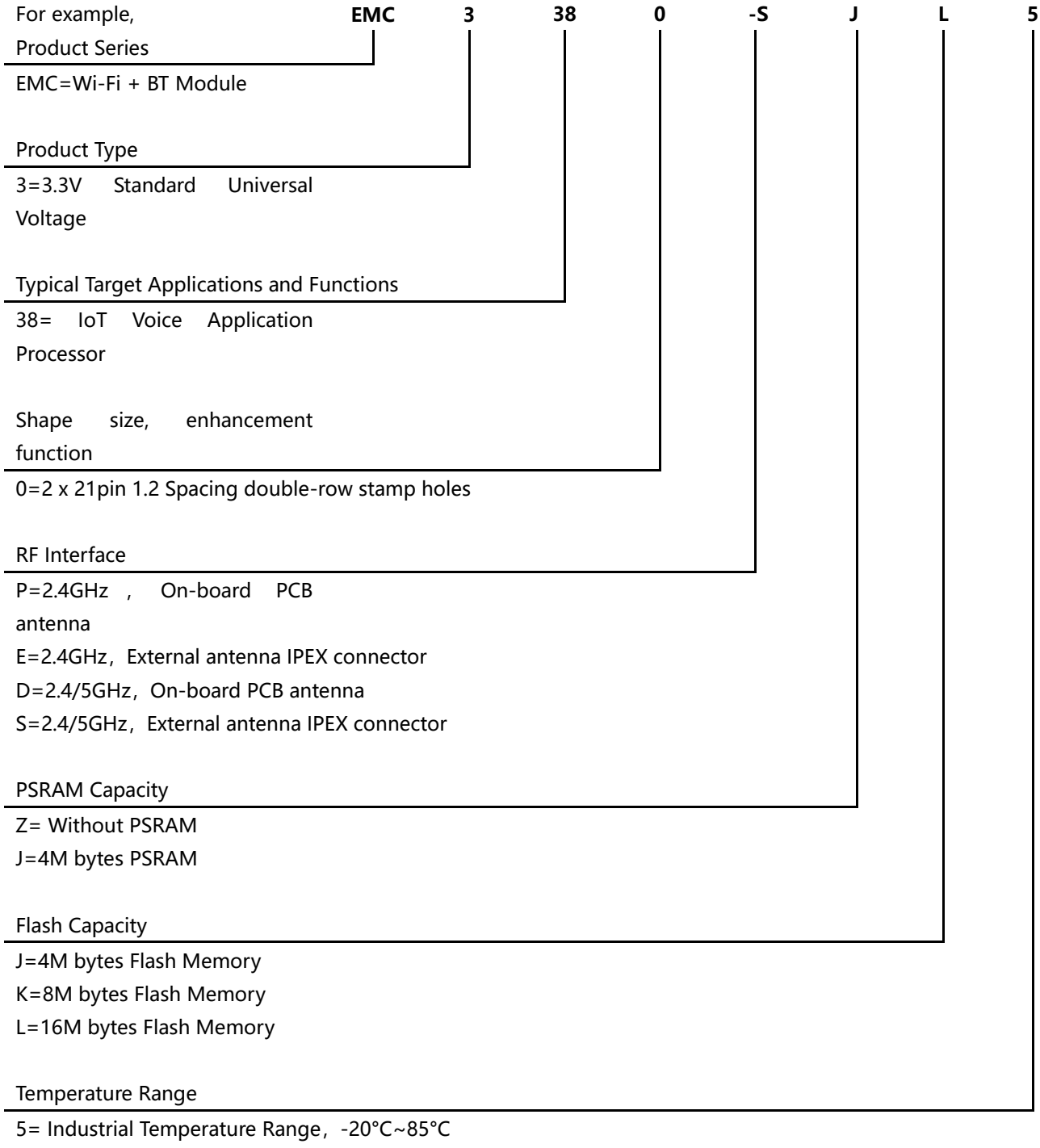
- **Peripherals**
  - 34 x GPIO
  - 1 x USB、3 x SPI、1 x I2C、1 x Infrared、11 x PWM
  - 3 x UART：
    ✓ 1 x Log UART、1 x LP UART、1 x HS UART
    ✓ The baud rate is as high as 4M.
  - Up to 7 channels 12-bit ADC, 1M sampling rate, battery power detection
  - Low power RTC (32kHz)
  - Up to 5 x 5 matrix keyboard and 4 touch keys can be supported

- **Operating Temperature：-20℃ to +85℃**
- **Antenna：On-Board PCB Antenna, or IPEX Connector**
- **Interface and Dimension**
  - EMC3380-E/S： 2 x 21pin 1.2pitch, double-row stamp hole

✓ EMC3380-E/S：external antenna，20mm x 27mm

✓ EMC3380-P/D: On-board Antenna，20mm x 33mm

Order Code



Optional model

Ordering Code	Description
EMC3380-SJL5	2.4/5GHz Dual Frequency Wi-Fi，BLE 5.0，External Antenna，4M bytes PSRAM, 16M bytes Flash
EMC3380-DJL5	2.4/5GHz Dual Frequency Wi-Fi，BLE 5.0，On-Board Antenna, 4M byte PSRAM, 16M byte flash memory
EMC3380-SJJ5	2.4/5GHz Dual Frequency Wi-Fi，BLE 5.0，External Antenna，4M bytes PSRAM, 4M bytes Flash
EMC3380-DJJ5	2.4/5GHz Dual Frequency Wi-Fi，BLE 5.0，On-Board Antenna, 4M byte PSRAM, 4M byte flash memory

Version Update Record

Date	Version	Update Items
2019-03-13	1.0	Initial Document.
2019-04-02	1.1	Update pin multiplexing.
2019-04-12	1.2	Update pin multiplexing table that increases function 7 and 8, and add internal pull-down.
2019-06-02	2.0	Update Document format, content to conform to the actual product.
2019-08-10	2.1	Add Module Label Information and Radio Frequency Part Data.
2019-09-12	2.2	Adjust the overall document format.
2020-02-26	3.1	Add dimension diagram
2020-11-23	3.2	Update order code and Low energy pin definition
2020-11-30	3.3	Update GPIO pin definition
2021-04-27	3.4	Add compliance information

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Catalog

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1. Introduction

EMC3380 is a high-performance module mainly used in voice applications of the Internet of Things. It has a dual-core microcontroller with ultra-high integration, supports 2.4/5GHz dual-band Wi-Fi and BLE 5.0 wireless communication technology, and includes large capacity Flash, RAM, audio codec and audio digital coprocessor to meet various complex requirements in speech application.

The core of high performance is a 32-bit core with a main frequency up to 200 MHz. Based on the latest ARM v8-M architecture, it not only has low power consumption, but also can complete floating-point operation and DSP instruction processing, thus completing the matching of audio coding and decoding algorithm and deep learning model efficiently. The core frequency of high energy efficiency reaches 20MHz, which provides a simplified instruction system for ultra-low power applications, so that the system can keep standby for a long time.

2.4/5GHz dual-band Wi-Fi guarantees stable Internet connection at any time. BLE 5.0 technology can not only facilitate users to complete the rapid configuration of products, but also realize the intelligent networking of a large number of local devices through Mesh technology.

The large capacity of Flash and RAM space allows developers to implement complex Internet of Things cloud service communication protocols, achieve long-term cache of high-resolution audio resources, and provide users with a perfect audio streaming media listening experience. The integrated dual microphone interface and audio front-end processing DSP chip can collect excellent voice resource samples for intelligent voice system, significantly reduce the algorithm complexity and improve the recognition rate of AI system. Rich peripheral interfaces can maximize system customization and expansion and facilitate the construction of innovative application products.

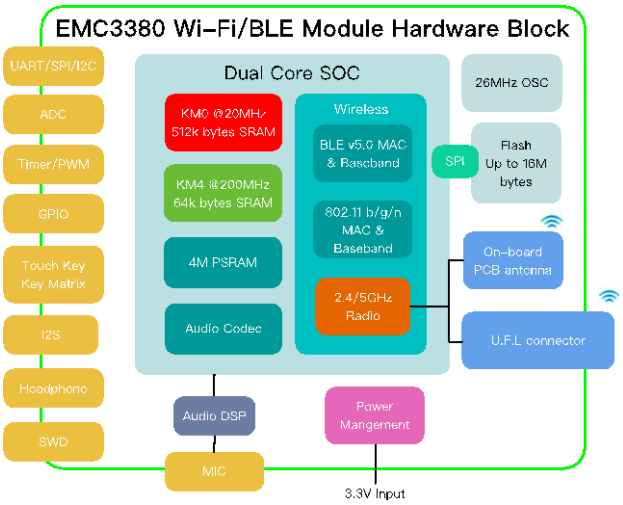
Shanghai MXCHIP provides MXOS software platform to support the development of EMC3380, providing an efficient development environment, rich sample programs and typical applications.

The following diagram is the hardware block diagram of EMC3380 module, which mainly includes:

- Dual-core wireless microcontroller
- Flash memory with optional capacity

- Optional Audio DSP Processing
- Plate-borne antenna or external antenna pedestal

Figure 1 EMC3380 Hardware Block Diagram



1.1. Peripheral List

Table 1 EMC3380 peripheral list

Item	Peripherals	Comment	Note
UART	HS_UART0		
	HS_UART1	Interior connect with Bluetooth	
	LP_UART1	Wake up in Low energy mode	
	LP_UART0	Log UART，Wake up in Low energy mode	
SPI	HS_SPI0	Support Master/Slave mode, Clock frequency up to 50MHz	
	HS_SPI1	Support Master mode, Clock frequency up to 25MHz	
	HS_USI_SPI	Support Master/Slave mode, Clock frequency up to 25MHz	
RTC	RTC_OUT		
	EXT_32K		
IR	IR		
I²C	LP_I2C	Standard mode (Max 100Kbps) Fast mode (Max 400Kbps)	
PWM	HS_PWM0 ~ 17		11route
	LP_PWM0 ~ 5	Support Low energy mode	6route
I²S	I²S		
DMIC	DMIC		
SGPIO	SGPIO		
Key-Scan	Key-Scan		7x3/5x5
Wake Pin	Wake Pin	Wake up from deepsleep mode	10pcs
LS_TIM4_TRIG	LS_TIM4_TRIG	Timer capture pin	
LS_TIM5_TRIG	LS_TIM5_TRIG	Timer capture pin	
HS_TIM4_TRIG	HS_TIM4_TRIG	Timer capture pin	
HS_TIM5_TRIG	HS_TIM5_TRIG	Timer capture pin	
Analog Pin	USB	USB Master/Slave mode, Master mode support mass storage	
	ADC	0 ~ 3.3V	7route
	VBAT_MEAS	Battery level detection	
	Audio Output	Audio analog output	x2(single ended)
	Audio Input	Audio analog output	x2(single ended)

2. Characteristics

2.1. System and Storage

Processor

- Dual-core processor
- KM4: Use ARM latest v8M architecture, compatible with Cortex-M4F instruction set
- KM4: Use ARM latest v8M architecture, compatible with Cortex-M0 instruction set
- Two cores have equal access to SRAM, peripherals and registers
- Internal communication between the two processors

KM4 processor

- Compatible with Cortex-M4F instruction set, support FPU, DSP, MPU and TrustZone-M technologies
- Working frequency up to 200MHz (configurable)
- SWD serial debugging interface, support 8 hardware breakpoints and 4 observation points (SWO interface function is not supported)
- Built-in NVIC interrupt vector table
- System tick timer.
- 32KB I-Cache and 4KB D-Cache.

K04 processor

Compatible with Cortex-M0 instruction set

Working frequency up to 20MHz

- Built-in NVIC interrupt vector table
- SWD serial debugging interface, support 4 hardware breakpoints and 2 observation points (SWO interface function is not supported)
- System tick timer.
- 32KB I-Cache and 4KB D-Cache

KM4 CPU On-Chip memory

- Up to 512KB continuous space main SRAM, frequency up to 200MHz
- Up to 4MB PSRAM, frequency up to 50MHz

KM4 CPU On-Chip memory

- Up to 64KB of continuous space main SRAM, frequency up to 64MHz
- Reserve 1KB SRAM for saving data in low power mode

GDMA

- KM4 and KM0 both include a GDMA controller.
- HS-GDMA0 supports 6 channels and supports TrustZone-M technology
- LP-GDMA0 supports 6 channels

Flash

- SPI Flash controller with cache
- Support ICP technology, directly program Flash

General-Purpose I/O (GPIO)

- 16 GPIOs with configurable pull-up and pull-down resistors
- Configurable external interrupt triggered by rising edge, falling edge and both edges

2.2. Wireless Communication

Wi-Fi

- 802.11 b / g / n 1x1, 2.4GHz & 5GHz
- Support 20MHz / 40MHz bandwidth, 802.11n rate reaches MCS7
- Low-power architecture, support low-power transmission and reception for short-range applications, low-power beacon monitoring mode, low-power RX mode, low-power suspend mode (DLPS)
- Support external power amplifier

BT BLE

- Support Bluetooth low energy
- Supports both master and slave modes
- High power mode (10dBm, sharing PA with Wi-Fi)
- Built-in Wi-Fi / Bluetooth single antenna coexistence mechanism

2.3. Security

- AES / DES / SHA hardware encryption algorithm engine
- Support TrustZone-M technology
- Support Secure boot
- SWD debug interface protection to prevent debug interface from accessing protected and prohibited areas
- Support RSIP, Flash data decryption

2.4. Communication Interface

USB

- Support USB 2.0, support high speed / full speed / low speed mode
- Support DMA transfer, 1.5Kbyte input block buffer, 1.5Kbyte output block buffer

SPI

- Support Motorola SPI serial data transmission
- Support master-slave mode
- Provide 2 SPI interfaces
- SPI0 (High speed): can be configured as master / slave mode, clock up to 50MHz.
- SPI1 (Normal speed): can be configured as master mode, clock up to 25MHz
- Support DMA transfer
- Configurable independent interrupt
- FIFO depth: The receive and transmit FIFO queues have a depth of 64 words, and each word has 16 bits.
- Hardware / software slave device selection function: You can use special hardware slave device chip select pins or use software to control GPIOs as chip select signals for SPI slave devices.
- Programmable features:
- Clock frequency: When set to master mode, the bit rate of data transmission can be controlled dynamically
- The size of each transmitted data (4 ~ 16 bits)
- Clock polarity and phase
- When set to receive serial data in master mode, the delay time of sampling can be set to achieve higher serial bit rate

UART

- Supported UART format: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bit
- Support hardware flow control
- Support interrupt control
- Support IrDA
- Support loopback mode for testing
- Support TX, RX use different clocks
- Tx channel can use a baud rate generator with decimals to generate accurate clock
- Rx channel supports low power mode
- Can monitor and eliminate the baud rate error and drift on the Rx channel

- Support DMA transfer

IR (Infra Ray)

- Support carrier frequency range: 25KHz to 500KHz, duty cycle: 1/2 to 1/5
- Support infrared diode input and infrared receiver module input
- 32 * 4 bytes Tx FIFO, 32 * 4 bytes Rx FIFO
- Can set carrier frequency and duty cycle

One wire (SGPIO)

- Single-line communication interface for secure encryption chip

I2C

- Two-wire I2C serial interface, consisting of data line (SDA) and clock line (SCL)
- Supports one I2C interface, supports two standard modes up to 100Kbps and high-speed modes up to 400Kbps, and supports clock stretching
- Support I2C master device or slave device
- Support 7-bit or 10-bit address addressing, and support mixed transmission
- Receive and transmit buffer with 16 word depth
- Support DMA for data transmission and reception
- Support bus arbitration mechanism to realize the communication capability of multi-master equipment
- Wake up from device address matching to achieve low power consumption
- Software configurable parameters: SDA hold time, slave device address, etc.
- Programmable digital filters for SDA and SCL signals for filtering noise on signal lines
- Can use the USI interface to build another I2C interface, supporting 400Kbps high-speed mode

2.5. Timer

Basic timers (HS_TIM0 ~ HS_TIM3, LP_TIM0 ~ LP_TIM3)

- Clock source: 32KHz, precision: 32 bits, counting mode: up counting
- Support interrupt trigger, wake up in sleep mode

PWM timer (HS_TIM5, LP_TIM5)

- Channel: HS_TIM5 x 11 and LP_TIM5 x 6
- Clock source: XTAL, precision: 16 bits, counting mode: up counting, frequency division: 8 bits
- 2 x input capture pins

- LP_TIM5 can work in low power mode

Pulse timer (HS_TIM4, LP_TIM4)

- Channel: HS_TIM5 x 11 and LP_TIM5 x 6
- Clock source: XTAL, precision: 16 bits, counting mode: up counting, frequency division: 8 bits
- Single pulse mode, selectable polarity in PWM mode
- 2 x input capture pins, which can generate interrupts

Real-time clock RTC

- Independent BCD counter
- Day / hour / minute / second, 12/24 hour clock
- Software programmable clock compensation
- An alarm that can be triggered by any combination of time domains and generates interrupts
- Digital calibration circuit
- Register write protection

2.6. Human-Computer Interface

Matrix keyboard

- 10 IO ports, support up to 7 x 3, 5 x 5 matrix keyboard scanning
- Number of configurable keyboard rows and columns
- Configurable scan clock, scan interval and release time
- Support interrupt trigger
- Provide 12-bit and 16-depth FIFO to save the key press and release events
- Supports low power loss, the key time can wake the CPU from low power mode

Touch button

- Support 4 touch sensor channels
- Automatic hardware channel scanning, programmable scanning cycle, quantity and cycle
- Differential or absolute threshold judgment mode (ETC)
- Automatic environmental capacitance tracking and calibration (ETC)
- Hardware automatic baseline initialization
- Automatic baseline and threshold updates for noisy environments
- Programmable button debounce function

- Each interrupt source can enable interrupts
- 4 * 12 bits FIFO
- Ultra-low power consumption

2.7. Analog Processing

ADC and voltage comparator

- Successive approximation register ADC converter with 12-bit precision
- Number of channels
- 3 external 3.3V channels
- 3 internal channels
- Configurable inputs: single-ended mode and differential mode
- Support DMA transfer
- Sampling trigger source: software, timer
- A low-power voltage comparator for measuring battery power
- Can trigger wake-up circuit

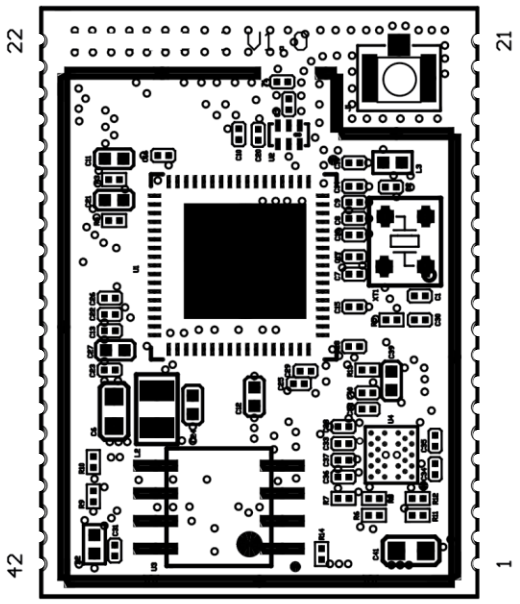
3. Pin Definition

3.1. Pin Distribution

EMC3380 has two sets of pins (1X21 + 1X21). Pin spacing is 1.2 mm.

The arrangement of the pins of EMC3380 is shown in Figure 2, and the pins are defined in Table 3.

Figure 2 EMC3380 Pin Arrangement



3.2. Pin Definition

3.2.1. General pin definition

Table 2 EMC3380 Pin Definition

Pin	Name (function after	Default State (2)	Function 1 (UART	Function 2	Function 3 (SPI)	Function 4	Function	Function 7 (I2C)	Function 9	Function 10	Function 12	Function 14	Function 15/PCM	Function	Function 22	ADC Channel
7	PA0	High-Z									I2S_SD_RX		QDEC_IDX	SGPIO		
9	PA2	High-Z									I2S_CLK		QDEC_PHB	SGPIO_OUT		
8	PA4	High-Z									I2S_WS		QDEC_PHA			
19	PA7(1) (UART_LOG_TXD)	Internal UP		UART_LOG_TXD												
20	PA8 (UART_LOG_RXD)	Internal UP		UART_LOG_RXD												

23	PA12[1]	High-Z	LP_UART_TXD		SPI1_MOSI				HS_PWM0	LP_PWM0	I2S_MCLK					
24	PA13[1]	EfusePullCtrl0	LP_UART_RXD		SPI1_MISO				HS_PWM1	LP_PWM1	I2S_SD_TX1					
25	PA14[1]	High-Z		LP_UART_RTS	SPI1_CLK						I2S_SD_TX2					
26	PA15[1]	EfusePullCtrl1		LP_UART_CTS	SPI1_CS											
27	PA16	High-Z		HS_UART0_RTS	SPI0_MOSI											
28	PA17	High-Z		HS_UART0_CTS	SPI0_MISO											
29	PA18	High-Z	HS_UART0_TXD		SPI0_CLK											
30	PA19	High-Z	HS_UART0_RXD		SPI0_CS						I2S_SD_TX0					
36	PA25	EfusePullCtrl2	LP_UART_RXD		HS_USI_SPI_MOSI		IR_TX	LP_I2C_SCL	HS_PWM4	LP_PWM4		HSDM				
35	PA26	High-Z	LP_UART_TXD		HS_USI_SPI_MISO		IR_RX	LP_I2C_SDA	HS_PWM5	LP_PWM5		HSDP				

31	PA27[1] (SWDIO)	Internal UP		LP_UART_RTS												
34	PA28	EfusePullCtrl3		LP_UART_CTS	HS_USI_SPI_CS				HS_PWM6	LP_PWM0		RREF				
33	PA30[1]	External UP			HS_USI_SPI_CLK				HS_PWM7	LP_PWM1		VBUS_OTG				
37	PB1[1]	EfusePullCtrl4	LP_UART_TXD								DMIC_CLK			SGPIO_OUT	HS_TIM4_TRIG	ADC4
42	PB2	High-Z	LP_UART_RXD								DMIC_DATA		PCM_CLK	SGPIO	HS_TIM5_TRIG	ADC5
32	PB3 (SWCLK)	High-Z											PCM_SYNC			ADC6
41	PB4	High-Z			SPI1_MOSI	RTC EXT_32K			HS_PWM8	LP_PWM2	I2S_SD_TX1		PCM_IN		HS_TIM4_TRIG	ADC0 TOUCH_KEY0
40	PB5	High-Z			SPI1_MISO	RTC_OUT		LP_I2C_SCL	HS_PWM9	LP_PWM3	I2S_SD_TX2		PCM_OUT		HS_TIM5_TRIG	ADC1 TOUCH_KEY1

39	PB6	High-Z			SPI1_CLK	LP_TIM4_TRIG		LP_I2C_SDA								ADC2 TOUCH_KEY2
38	PB7	EfusePullCtrl5			SPI1_CS	LP_TIM5_TRIG			HS_PWM17	LP_PWM5						ADC3 TOUCH_KEY3
4	PB22	EfusePullCtrl7	HS_USI_UART_TXD			LP_TIM4_TRIG	IR_RX	HS_USI_I2C_SCL	HS_PWM14	LP_PWM2	I2S_SD_RX		QDEC_PHB	SGPIO_OUT		
5	PB23(1)	High-Z	HS_USI_UART_RXD			LP_TIM5_TRIG	IR_TX	HS_USI_I2C_SDA	HS_PWM15	LP_PWM3	I2S_MCLK		QDEC_PHA	SGPIO_OUT		
6	PB26	High-Z									I2S_SD_TX0			SGPIO		
15	PB29	High-Z					IR_RX				I2S_CLK			SGPIO		
16	PB31	High-Z					IR_TX				I2S_WS		QDEC_PHA	SGPIO		
3	VBAT_MEAS															
18	nRESET		nRESET													

1	VDD		VDD													
2,21,22	GND		VSS													
17	AGND															
10	CLOC_SEL(3)															
11	BOOT_SEL(3)															
12	CHAN_SEL(3)															
13	ALPHA_SEL(3)															
14	VREG(3)															

(1). Special function capture pins. When the module starts, it will detect the state of these pins to enter special functions, please refer to section 3.2.3

(2). The default state of the pin. When the Reset button is pressed, all GPIO ports will maintain the previous state. When the Reset button is released, the state of the GPIO returns to the state described in "Default State" in Table 2. EfusePullCtrlx indicates that the default state of the pin is determined by the eFuse status bit is determined.

(3). The time from system power-on to GPIO power supply can be divided into three phases:

1. The power supply voltage rises to 1.5V, and the internal AON_LDO voltage rises to 0.5V. Determined by 3.3V / 1.8V power-on time

2. The chip's internal analog circuit needs 6ms to power the Reset button, and then the digital circuit starts to work.

3. After 300us ~ 1.5ms, the GPIO is powered on, and the default level takes effect.

Phases 2 and 3 take a total of 6.3ms to 7.5ms.

3.3. Low energy pin definition

Low energy pins can wake the module from DeepSleep state, and they are located on the keyboard scan function and touch function pins.

Table 3 Low energy pin definition

Pin Number	Name	Function 28 (Ext32K)	Function 29 (key scan row)	Function 30 (key scan col)	Function 31 (wakeup)	PX_FUNC_DEFAULT
14	PA12		KEY_ROW0		LGPIO0	GPIOC_LP0
15	PA13		KEY_ROW1		LGPIO1	GPIOC_LP1
19	PA14	RTC_OUT	KEY_ROW2		LGPIO2	GPIOC_LP2
23	PA15	RTC EXT_32K	KEY_ROW3	KEY_COL6	LGPIO3	GPIOC_LP3
	PA16		KEY_ROW4	KEY_COL5	LGPIO0	GPIOC_LP4
	PA17		KEY_ROW6	KEY_COL3	LGPIO1	GPIOC_LP5
	PA18		KEY_ROW5	KEY_COL4	LGPIO2	GPIOC_LP6
	PA19	RTC_OUT		KEY_COL2	LGPIO3	GPIOC_LP7
10	PA25			KEY_COL1	LGPIO2	GPIOC_LP10

9	PA26			KEY_COL0	LGPIO3	GPIOC_LP11

3.4. Special Function Capture Pin

The module will detect the status of these pins during power-on to enter some special modes and functions. These functions are determined by the hardware and cannot be modified.

Table 4 Special Function Capture Pin

Pin Name	Trap Function	State	Description
PA7	UART_DOWNLOAD	High (Default)	Boot application normally
		Low	Boot ROM code, enter Flash download mode
PA12	ICFG0	Test mode，ignore if not enter test mode	
PA13	ICFG1	Test mode，ignore if not enter test mode	
PA14	ICFG2	Test mode，ignore if not enter test mode	
PA15	ICFG3	Test mode，ignore if not enter test mode	
PA27	NORMAL_MODE_SEL	High (Default)	Boot application normally
		Low	Enter test mode, use A12 ~ PA15
PA30	SPS_SEL	High (Default)	SWR mode(Pull up 10K inside the module)
		Low	LDO mode

If the module firmware is developed using the MXOS development platform provided by MXCHIP, the application will also detect the status of the following pins during the boot process and enter a special working mode. These functions can be adjusted by modifying the code. The default functions are described below. Before final production, if these functions are useful, verification testing is required.

There are currently three working modes to choose from:

- Normal: Run the application normally.
- ATE: Runs the RF test mode. In this mode, you can test the RF transmit power and receive sensitivity and calibrate the RF parameters. Use UART_LOG (TX: PA7, RX: PA8) to interact with the ATE command.

- QC: Run the factory test mode, output QC information through LP_UART (TX: PB1, RX: PB2), and cooperate with the detection program running on the PC, which can be used to verify the firmware version in the module, the login information of the cloud service, and basic hardware Features.

When detecting the state of the pin, the firmware first sets the mode of PB1 and PB23 to input pull-up. Therefore, if there is no external interference, the read IO state is high, and the default working state is: Normal.

Table 5 Firmware special function capture pin

Firmware operation mode	PB1 (BOOT)	PB23 (STATUS)
Normal	1	Not test
ATE	0	1
QC	0	0

4. System memory Space

The EMC338x module contains the following memory cells:

4.1. KM4 Embedded SRAM

The KM4 core contains up to 512K bytes of continuous on-chip SRAM memory. The embedded SRAM is available in bytes (8 bits), half words (16 bits) or single words (32 bits). It is divided into two blocks, both of which can be accessed by the KM4 and KM0 cores.

- KM4 SRAM1 (up to 256KB)
- KM4 SRAM2 (up to 256KB)

Dividing SRAM into two sending device ports allows users' applications to obtain better performance. For example, it is possible to access the SRAM through the CPU and the DMA controller simultaneously without causing delay. Generally, when the DMA is reading and writing data from the peripheral to the SRAM, the CPU will also access the SRAM to read and write the data of other peripherals. Therefore, the reading and writing of different peripheral data is placed in different SRAM blocks Can reduce latency. In addition, SRAM is read and written alternately to access the same peripheral data sequence. For example, when the DMA is reading or writing to a RAM buffer and is ready to operate on the next buffer, the CPU is notified. In this way, the CPU and DMA can operate different buffers in different SRAM blocks at the same time, reducing access latency.

In the power supply area, the entire SRAM is also divided into 3 blocks:

- SRAM_PD1 (up to 256KB)
- SRAM_PD2 (up to 128KB)
- SRAM_PD3 (up to 128KB)

Each block can be individually enabled in the power management unit (PMU), and this SRAM can be restored as quickly as possible when the system wakes up from sleep mode.

4.2. KM0 Embedded SRAM

The KM0 core contains up to 64K bytes of memory. The embedded SRAM is available in bytes (8 bits), half words (16 bits) or single words (32 bits) and accessible by KM4 and KM0 cores.

4.3. KM4 Extension SRAM

If Bluetooth is not used, the KM4 core can be expanded with an additional 64KB of SRAM. This SRAM can also be accessed through KM4 and KM0 at speeds up to 50MHz * 32 bits.

4.4. Retention SRAM

The chip also provides 1KB of SRAM, which is used to save data with the lowest power consumption in deepsleep mode. This SRAM can also be accessed by KM4 and KM0.

4.5. SPI Flash Memory

The CPU manages access to flash memory from the I-Code and D-Code buses via the built-in SPI Flash Control Unit (SPIC). At the same time, operations such as erasure, programming, and read-write protection are also implemented, and the execution of code stored in flash memory is accelerated by instruction prefetch and cache.

4.6. PSRAM

4M bytes PSRAM, using 50MHz DDR memory.

4.7. System storage control address allocation

Address allocation is as following table.

Table 6 System storage space

Base Address	Top Address	Size	Function	Description
0x0000_0000	0x0001_FFFF	128KB	KM0 ITCM ROM (actually 96KB)	32MB: KM0 Memory Address
0x0002_0000	0x0002_7FFF	32KB	KM0 DTCM ROM (actually 16KB)	
0x0002_8000	0x0007_FFFF	352KB	RSVD	
0x0008_0000	0x0008_FFFF	64KB	KM0 SRAM	
0x0009_0000	0x000B_FFFF	192KB	RSVD	
0x000C_0000	0x000C_3FFF	16KB	Retention	

			SRAM (1KB) (the same port with KM0 SRAM)	
0x000C_4000	0x000F_FFFF	240KB	RSVD	
0x0010_0000	0x01FF_FFFF	31MB	RSVD	
0x0200_0000	0x07FF_FFFF	96MB	PSRAM	224MB: External Memory Address
0x0800_0000	0x0FFF_FFFF	128MB	External FLASH	
0x1000_0000	0x1007_FFFF	512KB	KM4 SRAM	256MB: KM4 Memory Address
0x1008_0000	0x100D_FFFF	384KB	RSVD	
0x100E_0000	0x100E_FFFF	64KB	Extension SRAM0 from Bluetooth	
0x100F_0000	0x100F_FFFF	64KB	Extension SRAM1 from Wi-Fi	
0x1010_0000	0x1013_FFFF	256KB	KM4 ITCM ROM	
0x101C_0000	0x101D_7FFF	96KB	KM4 DTCM ROM	
0x101E_0000	0x101F_FFFF	256KB	RSVD	
0x1020_0000	0x1FFF_FFFF	254MB	RSVD	
0x2000_0000	0x3FFF_FFFF	512MB	RSVD	Reserved
0x4000_0000	0x47FF_FFFF	128MB	KM4 Peripherals	128MB: KM4 Peripherals Address
0x4800_0000	0x4FFF_FFFF	128MB	KM0 Peripherals	128MB: KM0 Peripherals Address
0x5000_0000	0x57FF_FFFF	128MB	KM4 Peripherals Secure	128MB: KM4 Peripherals Secure

				Address
0x5800_0000	0xFFFF_FFFF	2816MB	RSVD	Reserved

Partition the flash storage space to store firmware and data for different functions. When using the MXOS platform provided by MXCHIP to develop firmware, the 4MB Flash space is pre-allocated as follows. When using other development environments or different Flash capacities, please refer to the relevant technical description.

Table 7 MXOS 4M byte Flash storage space partition

Name	Description	Start Address	Size
KM0 Boot	KM0 core boot loader	0x0800_0000	20 Kbytes
Backup	System data backup area	0x0800_2000	4 Kbytes
System Data	System Data	0x0800_3000	4 Kbytes
KM4 Boot	KM4 Core Bootloader	0x0800_4000	8 Kbytes
APP1	Application partition 1, when OTA upgrade, switch with APP2 to boot.	0x0800_6000	1504 Kbytes
KV	Key/Value Data Storage Area	0x0817_E000	16 Kbytes
BT FTL	Bluetooth Binding Information Storage Area	0x0818_2000	12 Kbytes
APP2	Application partition 2, when OTA upgrade, switch with APP 1 to boot.	0x0818_8000	1504 Kbytes
USER	User uses partition	0x0830_0000	1024 Kbytes

KM0 Boot, KM4 Boot, and APP1 are necessary parts for system operation.

5. Electrical Parameters

5.1. Absolute Maximum Parameter

Modules operating outside the absolute maximum ratings may cause permanent damage. At the same time, long-term exposure to the maximum rating conditions will affect the reliability of the module.

Table 8 Absolute maximum parameter: voltage

Symbol	Ratings	Min	Max	Unit
VDD–VSS	Voltage	–0.3	3.6	V
VIN	Input voltage on any other pin	VSS−0.3	VDD+0.3	V

5.2. Operation Voltage and Current

Table 9 operating parameter: voltage and current

Symbol	Note	Specification			
		Min.	Typical	Max.	Unit
V_{DD}	Voltage	3.0	3.3	3.6	V
I_{VDD}	3.3V Rating Current (with internal regulator and integrated CMOS PA)			450	mA

Table 10 Average power consumption under 3.3V

Operation Mode		Conditions	Average Current	Unit
Power Mode	Scenario			
Deepsleep	Deepsleep	RTC timer 1KB retention RAM	7~8	μA
	Deepsleep with Key-Scan	RTC timer 1KB retention RAM Key-Scan	12~13	μA

Operation Mode		Conditions	Average Current	Unit
Power Mode	**Scenario**			
	Deepsleep with Cap-Touch (average current)	RTC timer 1KB retention RAM Cap-Touch	20	µA
Sleep	WoWLAN sleep power	KM4 power gate KM0 clock gate All RAM retained Wi-Fi retained	30~50	µA
Active	Wi-Fi Rx Idle	HT20 MCS0~7 normal mode KM4 in active mode Rx idle	81	mA
		HT20 MCS0~7 ultra-low power mode KM4 in active mode Rx idle	60	mA
	Wi-Fi Rx UDP	HT20 MCS0~7 ultra-low power mode KM4 in active mode UDP Rx @ 8Mbps	67	mA
WoWLAN	WoWLAN Rx Beacon	Rx beacon mode @ normal mode KM4 in sleep mode	45	mA
		Rx beacon mode @ ultra-low power mode KM4 in sleep mode	39	mA
	WoWLAN DTIM=1 (Average)	KM4 in sleep mode All SRAM retained Wi-Fi retained	1.1~2	mA

Operation Mode		Conditions	Average Current	Unit
Power Mode	Scenario			
		Open space		

Table 11 RF consumption under 3.3V

Operation Mode	Current		Unit
	2.4G	5G	
1T-MCS7/BW40M (15dBm)	206	286	mA
1T-MCS7/BW40M (18dBm@2.4G, 17dBm@5G)	247	310	
1T-MCS7/BW20M (15dBm)	204	286	
1T-MCS7/BW20M (18dBm)	248	308	
1T-Legacy_OFDM54M (16dBm)	214	296	
1T-Legacy_OFDM54M (19dBm@2.4 18dBm@5G)	262	323	
1T_CCK11M (18dBm)	257		
1T_CCK11M (21dBm)	312		
1R-Idle/BW40	52	53	
1R-MCS7/BW40M (Pin= -60dBm)	61	64	
1R-MCS7/BW20M (Pin= -60dBm)	62	63	
1R-Legacy_OFDM54M (Pin= -60dBm)	61	62	
1R-CCK11M (Pin= -60dBm)	52		
RF Standby	24	23	
RF Disable	24	23	

5.3. Digital IO DC characteristic

The electrical characteristics of the module's digital IO port are described in Table 12

under 3.3V power supply.

Table 12 operation parameter（3.3V）:Digital IO DC characteristic

Symbol	Note	Conditions	Specification			
			Min.	Typical	Max.	Unit
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	9.58	9.59	13.43	V
V_{OL}	Output-Low Voltage	LVTTL			0.4	V
I_{IL}	Input-Leakage Current	V_{IN} = 3.3V/0V	-10	±1	10	μA

5.4. Temperature

Table 13 Storage temperature and operation temperature

Symbol	Ratings	Min.	Max	Unit
T_{STG}	Storage temperature	−55	125	℃
T_A	Ambient Operating Temperature	-20	85	℃
T_J	Junction Temperature	0	125	℃

6. RF Parameter

6.1. Basic RF Parameters

Table 14 RF Standard

Item		Description
Operating Frequency Range (Dual Frequency)		2.4G Frequency Band：2400~24835GHz ; 5G Frequency Band：5150~5850MHz
Wireless standard		WIFI: IEEE802.11b/g/n(2.4G), 802.11a/n(5G)　Bluetooth: BLE5.0
Modulation Mode		Wi-Fi: 11b: DBPSK, DQPSK,CCK for DSSS 11g/a/n: BPSK, QPSK, 16QAM, 64QAM for OFDM Bluetooth: GFSK
Data transmission rate of theoretical physics	20MHz	11b：1,2,5.5,11Mbps 11g /a: 6,9,12,18,24,36,48,54Mbps 11n_HT20: MCS0~7, Maximus 65Mbps
	40MHz	11n_HT40(2.4G&5G): MCS0~7, Maximum 135Mbps
	2MHz	BLE_1Mbps BLE_2Mbps
Antenna Type		IPEX External Antenna Onboard PCB Antenna

6.2. EMC3380 Wi-Fi RF characteristics

6.2.1. IEEE 802.11b mode

Table 15 EMC3380 IEEE 802.11b TX/RX characteristics

Item	Description			
Mode	IEEE802.11b			
Channel	CH1 to CH13			
Data Rates	1, 2, 5.5, 11Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				

11b Target Power@1Mbps	15.0	16.5	18.0	dBm
11b Target Power@11Mbps	15.0	16.5	18.0	dBm
Spectrum Mask @ target power				
fc +/-11MHz to +/-22MHz	-	-	-30	dB
fc > +/-22MHz	-	-	-50	dB
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
1~11Mbps	-	-	35% (or -11dB)	
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
1Mbps (FER≦8%)	-	-98	-	dBm
11Mbps (FER≦8%)	-	-88	-	dBm

6.2.2. IEEE802.11g mode

Table 16 EMC3380 IEEE802.11g TX/RX characteristics

Item	Description			
Mode	IEEE802.11g			
Channel	CH1 to CH13			
Data Rates	6, 9, 12, 18, 24, 36, 48, 54Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				
11g Target Power@6Mbps	13.5	15.0	16.5	dBm
11g Target Power@54Mbps	13.0	14.5	16	dBm

Spectrum Mask @ target power				
fc +/- 11MHz	-	-	-20	dB
fc +/- 20MHz	-	-	-28	dB
fc > +/-30MHz			-40	dB
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
6Mbps	-	-30	-5	dBm
54Mbps	-	-30	-25	dBm
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
6Mbps (FER≦10%)	-	-93	-	dBm
54Mbps (FER≦10%)	-	-76	-	dBm

6.2.3. IEEE802.11n-HT20(2.4G) mode

Table 17 EMC3380 IEEE802.11n-HT20 TX/RX characteristics

Item	Description			
Mode	IEEE802.11n HT20			
Channel	CH1 to CH13			
Data Rates	MCS0/1/2/3/4/5/6/7, up to 65Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				
11n Target Power@MCS0	13.5	14.5	16	dBm
11n Target Power@ MCS7	12.5	14	15.5	dBm

Spectrum Mask @ target power				
fc +/- 11MHz	-	-	-20	dB
fc +/- 20MHz	-	-	-28	dB
fc > +/-30MHz			-45	dB
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
MCS0	-	-30	-5	dBm
MCS7	-	-31	-27	dBm
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
MCS0 (FER≦10%)	-	-93	-93	dBm
MCS7 (FER≦10%)	-	-73.5	-73	dBm

6.2.4. IEEE802.11n-HT40(2.4G) mode

Table 18 EMC3380 IEEE802.11n-HT40 TX/RX characteristics

Item	Description			
Mode	IEEE802.11n HT40			
Channel	CH1 to CH13			
Data Rates	MCS0/1/2/3/4/5/6/7, up to 135Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				
11n Target Power@MCS0	13.5	14.5	16	dBm
11n Target Power@ MCS7	12.5	14	15.5	dBm
Spectrum Mask @ target power				

fc +/- 22MHz	-	-	-20	dB
fc +/- 40MHz	-	-	-28	dB
fc > +/-60MHz	-	-	-45	dB
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
MCS0	-	-30	-5	dBm
MCS7	-	-32	-27	dBm
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
MCS0 (FER≦10%)	-	-90	-	dBm
MCS7 (FER≦10%)	-	-71.5	-	dBm

6.2.5. IEEE802.11a mode

Table 19 EMC3380 IEEE802.11a TX/RX characteristics

Item	Description			
Mode	IEEE802.11a			
Channel	CH36 to CH165			
Data Rates	6, 9, 12, 18, 24, 36, 48, 54Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				
11g Target Power@6Mbps	12.5	14	15.5	dBm
11g Target Power@54Mbps	11.5	13	14.5	dBm
Spectrum Mask @ target power				
fc +/- 11MHz	-	-	-20	dBr

fc +/- 20MHz	-	-	-28	dBr
fc > +/-30MHz			-40	dBr
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
MCS0	-	-29	-5	dBm
MCS7	-	-29	-25	dBm
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
6Mbps (FER≦10%)	-	-89	-	dBm
54Mbps (FER≦10%)	-	-74.5	-	dBm

6.2.6. IEEE802.11n HT20(5G) mode

Table 20 EMC3380 IEEE802.11n-HT20(5G) TX/RX characteristics

Item	Description			
Mode	IEEE802.11n(5G) HT20			
Channel	CH36 to CH165			
Data Rates	MCS0/1/2/3/4/5/6/7, up to 65Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				
11n Target Power@MCS0	11.5	13	14.5	dBm
11n Target Power@MCS7	10.5	12	13.5	dBm
Spectrum Mask @ target power				
fc +/- 11MHz	-	-	-20	dB
fc +/- 20MHz	-	-	-28	dB

fc > +/-30MHz	-	-	-45	dB
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
MCS0	-	-28	-5	dBm
MCS7	-	-30	-27	dBm
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
MCS0 (FER≦10%)	-	-92.5	-	dBm
MCS7 (FER≦10%)	-	-72	-	dBm

6.2.7. IEEE802.11n HT40(5G) mode

Table 21 EMC3380 IEEE802.11n-HT40(5G) TX/RX characteristics

Item	Description			
Mode	IEEE802.11n(5G) HT40			
Channel	CH36 to CH165			
Data Rates	MCS0/1/2/3/4/5/6/7, up to 135Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				
11n Target Power@MCS0	11.5	13	14.5	dBm
11n Target Power@MCS7	10.5	12	13.5	dBm
Spectrum Mask @ target power				
fc +/- 11MHz	-	-	-20	dBr
fc +/- 20MHz	-	-	-28	dBr

fc > +/-30MHz			-45	dBr
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
MCS0	-	-28	-5	dBm
MCS7	-	-30	-27	dBm
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
MCS0 (FER≦10%)	-	-89	-	dBm
MCS7 (FER≦10%)	-	-69	-	dBm

6.3. Bluetooth RF characteristic

Table 22 EMC3380 BLE4.0 TX/RX Characteristics Parameters

Item	DataRate	Min	Typical	Max	Remark
POWER_AVERAGE	LE_1M	6	10	10dBm	
Frequency Drift Error	LE_1M	-50KHz	-5	50KHz	
Carrier frequency offset and drift at NOC:					
ΔFn max	LE_1M	-150KHz	6.1	150KHz	
|F0-Fn|	LE_1M		2.37	50KHz	
|F1-F0|	LE_1M		2.1	20KHz	
|Fn-Fn5|	LE_1M		0.89	20KHz	
Modulation characteristics:					
ΔF1avg	LE_1M	225KHz	249	275KHz	
ΔF2avg	LE_1M	185KHz	238	275KHz	
ΔF2avg/ΔF1avg	LE_1M	0.8	0.96		
ΔF2max	LE_1M	185KHz	245		
In-Band Emissions					
OFFSET_-2	LE_1M		-44.3	-20dBm	
OFFSET_-3	LE_1M		-46.6	-30dBm	

OFFSET_-4	LE_1M		-46.5	- 30dBm	
OFFSET_-5	LE_1M		-50.6	- 30dBm	
OFFSET_2	LE_1M		-46.1	- 20dBm	
OFFSET_3	LE_1M		-45.7	- 30dBm	
OFFSET_4	LE_1M		-44.4	- 30dBm	
OFFSET_5	LE_1M		-50.2	- 30dBm	
RX Characteristics					
Minimum Sensitivity	LE_1M	-	-98dBm	-97dBm	PER ≤30.8%

Table 23 EMC3380 BLE5.0 TX/RX Characteristics Parameters

Item	Datarate	Min	Typical	Max	Remark
POWER_AVERAGE	LE_2M	4	8	10dBm	
Frequency Drift Error	LE_2M	-50KHz	-4.3	50KHz	
Carrier frequency offset and drift at NOC:					
ΔFn max	LE_2M	-150KHz	6.1	150KHz	
|F0-Fn|	LE_2M		2.37	50KHz	
|F1-F0|	LE_2M		2.1	23KHz	
|Fn-Fn5|	LE_2M		0.89	20KHz	
Modulation characteristics:					
ΔF1avg	LE_2M	450KHz	502.1	550KHz	
ΔF2avg	LE_2M	450KHz	499.7	550KHz	
ΔF2avg/△F1avg	LE_2M	0.8	0.995		
ΔF2max	LE_2M	370KHz	509		
In-Band Emissions					
OFFSET_-4	LE_2M		-47.01	-20dBm	
OFFSET_-5	LE_2M		-50.95	-20dBm	

OFFSET_-6	LE_2M		-50.95	- 30dBm	
OFFSET_4	LE_2M		-45.85	- 20dBm	
OFFSET_5	LE_2M		-50.75	- 20dBm	
OFFSET_6	LE_2M		-50.75	- 30dBm	
RX Characteristics					
Minimum Sensitivity	LE_2M	-	-98dBm	-97dBm	PER ≤30.8%

7. Antenna Information

7.1. Antenna Type

EMC3380 has two specifications: PCB antenna and IPX connector. Please refer to order code.

Table 24 EMC3380 Onboard PCB antenna parameter (2.4GHz)

Item	Min.	Typical	Max.	Unit
Frequency	2400		2500	MHz
Impedance		50		Ω
VSWR			2	
Gain	-0.37dBi			
Efficiency	47%			

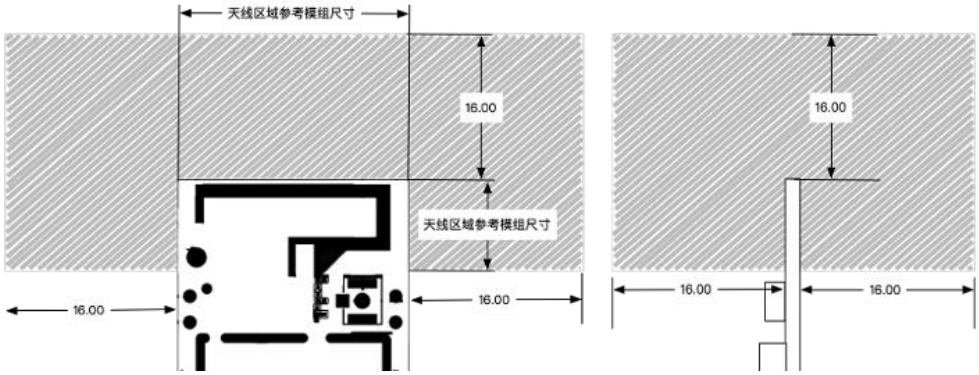
Table 25 EMC3380 Onboard PCB antenna parameter (5GHz)

Item	Min.	Typical	Max.	Unit
Frequency	5100		5800	MHz
Impedance		50		Ω
VSWR			2	
Gain	-0.69dBi			
Efficiency	42%			

7.2. PCB Antenna Clearance

When using PCB antenna in WIFI module, it is necessary to ensure that PCB and other metal devices are at least 16 mm away from the motherboard. The shaded areas in the figure below need to be far away from metal devices, sensors, interference sources and other materials that may cause signal interference.

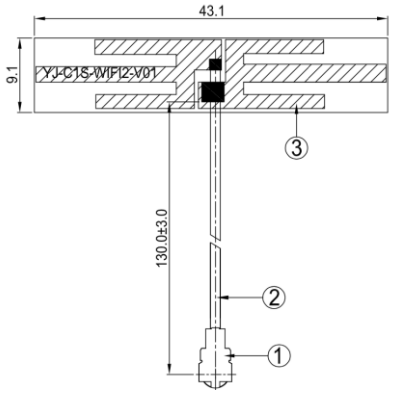
Figure 3 PCB Antenna Minimum Clearance（unit: mm）



7.3. External Antenna Connector

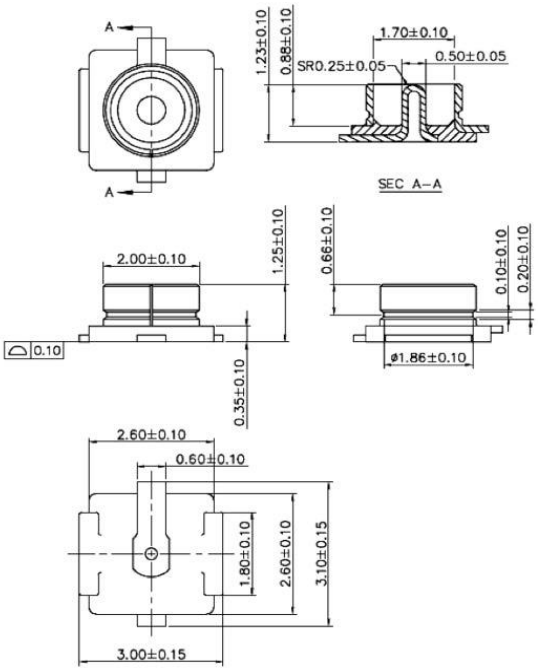
Users can select 2.4G & 5G antennas with different external dimensions and gains of no more than 2dBi depending on the application environment. The following is a copper tube antenna for an IPEX connector commonly used by MXCHIP.

Figure 4 Eternal antenna size



- Frequency Range: 2.4-2.5GHz 5.15-5.85GHz z
- Input independence: 50 Ohm
- SWR: < 2.0
- Gain： 3.0dBi@2.4-2.5GHz 5.9dBi@5.15-5.85GHz
- Polarization: vertical
- Directionality: Omnidirectional
- Copper tube: 4.4*23mm: 4.4*23mm
- RL: < -10 dB
- Cable: O.D.1.13mm//L=130mm, Blue

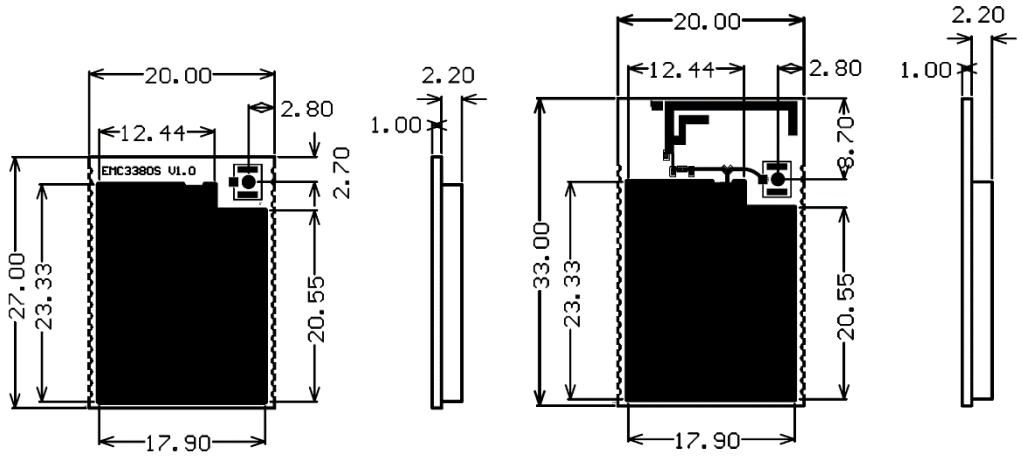
Figure 5 Dimension Diagram of External Antenna Connector



8. Dimensions and Production Guidance

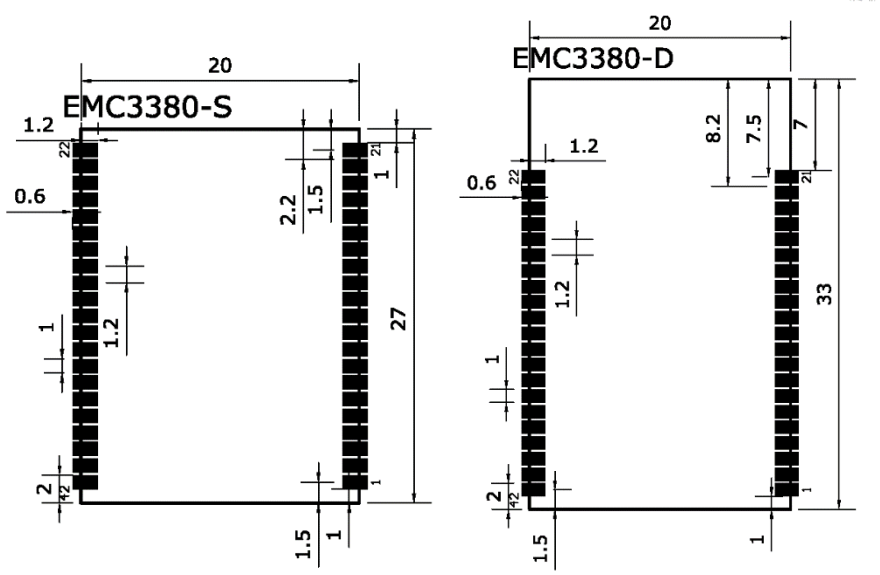
8.1. Assembly Dimension Diagram

Figure 6 EMC3380-S, EMC3380-D dimension（unit: mm）



8.2. Packing dimension diagram

Figure 7 EMC3380-S, EMC3380-D packing dimension（unit: mm）



Note: All dimensional tolerances marked in the figure are ± 0.25mm.

9. Production Guidelines

MXCHIP stamp port packaging module must be SMT machine patches, module humidity sensitivity grade MSL3, after unpacking more than a fixed time patches to bake module.

- SMT patches require instruments
  - Reflow bonding machine
  - AOI detector
  - 6-8mm suction nozzle
- Baking requires equipment:
  - Cabinet oven
  - Anti-static, high temperature tray
  - Antistatic and heat resistant gloves

The storage conditions of MXCHIP module are as follows:

- Moisture-proof bags must be stored in an environment with temperature < 30 degree C and

  humidity < 85% RH.
- A humidity indicator card is installed in the sealed package.

Figure 8 Humidity Card

After the module is split, if the humidity card shows pink, it needs to be baked.

The baking parameters are as follows:

- The baking temperature is 120℃±5℃ and the baking time is 4 hours.

- The alarm temperature is set to 130℃.
- SMT patches can be made after cooling < 36℃ under natural conditions.
- Drying times: 1 time.
- If there is no welding after baking for more than 12 hours, please bake again.

If the disassembly time exceeds 3 months, SMT process is forbidden to weld this batch of modules, because PCB gold deposition process, over 3 months, pad oxidation is serious, SMT patch is likely to lead to virtual welding, leak welding, resulting in various problems, our company does not assume the corresponding responsibility;

Before SMT patch, ESD (Electrostatic Discharge, Electrostatic Release) protection should be applied to the module.

SMT patches should be made according to the reflow curve. The peak temperature is 250 C. The reflow temperature curve is shown in Chapter 9, Figure 10.

In order to ensure the qualified rate of reflow soldering, 10% of the first patches should be taken for visual inspection and AOI testing to ensure the rationality of furnace temperature control, device adsorption mode and placement mode, and 5-10 patches per hour are recommended for visual inspection and AOI testing in subsequent batch production.

9.1. Precautions

- Operators of each station must wear static gloves during the entire production process;
- Do not exceed the baking time when baking;
- It is strictly forbidden to add explosive, flammable or corrosive substances during baking;
- When baking, the module uses a high temperature tray to be placed in the oven to keep the air circulation between each module while avoiding direct contact between the module and the inner wall of the oven;
- When baking, please close the oven door to ensure that the oven is closed to prevent temperature leakage and affect the baking effect.
- Try not to open the door when the oven is running. If it must be opened, try to shorten the time for opening the door;

- After baking, the module should be naturally cooled to <36°C before wearing the static gloves to avoid burns;
- When operating, strictly guard against water or dirt on the bottom of the module;

The temperature and humidity control level of MXCHIP factory module is Level3, and the storage and baking conditions are based on IPC/JEDEC J-STD-020.

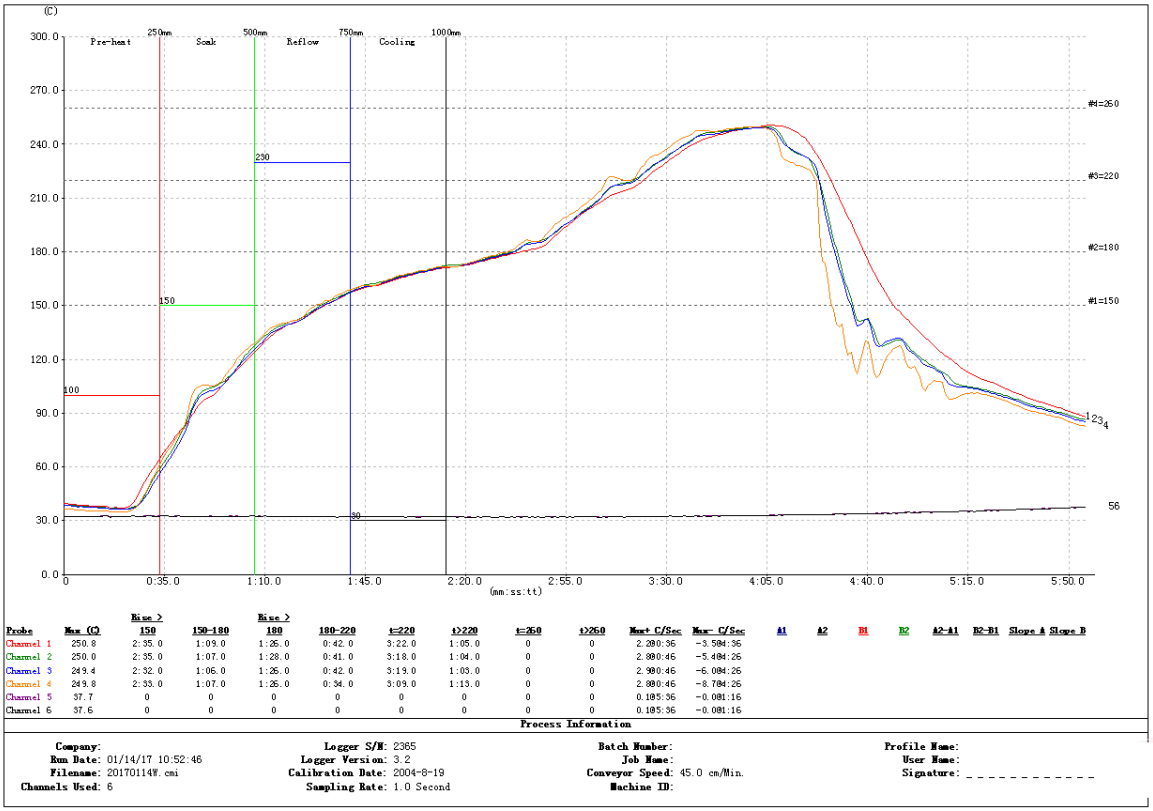
9.2. Storage Condition

Figure 9 Storage Conditions Diagram

9.3. Secondary Reflux Temperature Curve

We recommend solder paste model: SAC305, lead-free. No more than 2 reflux times.

Figure 10 Reference Secondary Reflux Temperature Curve



10. Compliance Information

10.1. FCC Information

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

The device has been evaluated to meet general RF exposure requirement. The device can be used in portable exposure condition without restriction. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

RF exposure considerations

This module complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body." This module is designed to comply with the FCC statement, FCC ID is: P53-EMC3280

Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for the specific rule parts. The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the host product being Part 15 Subpart B compliant (when it also

contains unintentional-radiator digital circuity), the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This module without unintentional-radiator digital circuity, so the module does not require an evaluation by FCC Part 15 Subpart B. The host should be evaluated by the FCC Subpart B.

10.2. EU Compliance Statement

This module is restricted to OEM installation only. When installing this module permanently into a host product to a create new radio equipment device; the manufacturer responsible for placing the final radio product on the market in the EU must assess if the combination of this radio module and the host product complies with the essential requirements of the RE Directive 2014/53/EU.

11. Label Information

Figure 11 Module Label Schematic Diagram

1. MXCHIP: Company Logo.
2. CMIIT ID: SRRC Model Authorization ID, 10 bits, not yet available, replaced by X.
3. EMC3380-S: Product Main Type.
4. JL5: Product Auxiliary Model.
5. X1916: Production serial number, where: X-factory code, 19-year of production, 16-week.
6. B0F893100008: MAC Address.
7. 0000.0000.A213: Firmware Number.

12. Sales and Technical Support Information

If you need to consult or purchase this product, please call Shanghai MXCHIP Information Technology Co., Ltd. during office hours.

Office hours: Monday to Friday morning: 9:00-12:00, afternoon: 13:00-18:00

Contact Tel: +86-21-52655026

Address: 9th Floor, Lane 5, 2145 Jinshajiang Road, Putuo District, Shanghai

Zip code: 200333

Email: sales@mxchip.com