MXCHIP®

Datasheet

EMC3280 Wi-Fi/BLE IoT Module

Built-in ARM Cortex V8 dual-core wireless processor, large capacity Flash memory and SRAM. 2.4 Hz Wi-Fi Internet Access and BLE 5.0 SIG Mesh Networking

Version：2.3　　Date：2021-11-30　　Number：DS0145EN

Abstract

- **Input Voltage：3.0V~3.3V**
- **Processor：Dual Core CPU with ARM v8-M architecture.**
  - Performance Core KM4：Cortex-M33，Main frequency up to 200 MHz.
  - Energy Efficiency Core KM0：Cortex-M23，Main frequency up to 20 MHz.
  - Deep Sleep、Deep Standby and Sleep mode.
  - SWD/JTAG Simulation Debug Interface.
- **Memory**
  - 512K bytes SRAM for KM4 core
  - 64K bytes SRAM for KM0 core
  - XIP flash memory from 2M to 8M bytes
  - Selection of Large Capacity PSRAM Storage
- **Wi-Fi**
  - IEEE 802.11 b/g/n 1T1R 2.4GHz Single frequency
  - Processing Wi-Fi messages using independent Microcontrollers.
  - Support low power TX/RX mode in short distance applications.
  - Support narrow-band mode: 10MHz bandwidth.
  - Support Antenna diversity.
  - Support IEEE Power Save Model
- **BT 5.0 Low Energy**
  - Comply with Low Power Bluetooth 5.0 Standard.
  - Support high power mode (10dbm).
  - Wi-Fi and BLE time division multiplexing and share the same PA and antenna.
  - Support Bluetooth Master-Slave Mode and BLE mesh.
- **Safety**
  - ARM Trust Zone-M Technology.
  - AES/SHA Hardware Accelerator, Random Number Generator

  - Security Boot Safe Start
  - Anti-reading mechanism: JTAG interface protection, flash encryption technology.
- **Peripherals**
  - 16 x GPIO (6 x Wakeup Pins, 3 x ADC channel)
  - 1 x SPI、1 x I²C、8 x PWM、5 x Timer
  - 2 x UART，Supporting Hardware Flow Control.
  - 1 x USI，can be set as UART、SPI or I²C
  - Infrared Transceiver
  - DMIC Digital Microphone Interface
  - SGPIO Single Line Communication
  - 4x2/3x3 Matrix Keyboard
  - USB Host/Device
- **Operating Temperature：-20℃ to +85℃**
- **Antenna：On-Board PCB Antenna, or IPEX Connector**
- **Applications and Functions**
  - Support AliOS Operating System and MXOS Development Platform
  - Provide access to major cloud platforms and Bluetooth Mesh networking protocol stack
  - Bluetooth/Wi-Fi Gateway Device for Internet of Things Applications
- **Interfaces and Dimensions**
  - Maintain pin compatibility with similar packaging modules
  - 18mm x 33mm, stamp hole or pin
  - Support external antenna or onboard antenna

Order Code

For example, **EMC 3 28 0 -P Z J 5**

Product Series

EMC=IoT Wi-Fi/BLE Combo Module

Product Type

3= Welding Wireless Module

Typical Target Applications and Functions

28=IOT Gateway Application, 8 Series Master Control

Shape size, enhancement function

0 = 18mm x 33mm，2 x 6pin 2.0 Spacing double-row stamp holes + 9 pin 2.0 spacing stamp holes or pins

RF Interface

P=2.4GHz Single Frequency，On-Board PCB Antenna

E=2.4GHz Single-frequency, external antenna IPEX connector

PSRAM Compacity(Optional)

Z=No PSRAM

J=4M bytes PSRAM

Flash Compacity

J=4M bytes Flash memory

K=8M bytes Flash memory

Temperature Range

5=Industrial Temperature Range， -20°C~85°C

Optional model

Order Code	Description
EMC3280-PZJ5	18mm x 33mm Stamp holes or Pinhole interface，On-board PCB Antenna，4M bytes flash，-20°C~85°C
EMC3280-EZJ5	18mm x 33mm Stamp holes or Pinhole interface， External Antenna pedestal ，4M bytes flash，-20°C~85°C

Parts

Order Code	Description
MXKIT-Base	Development board motherboard, suitable for all EMC328x modules
MXKIT-Core-C3280	Suitable for EMC3285 development board core board, including EMC3280-PZJ5 module. Matching with MXKIT-Base.
FX-C3280	EMC3280 manufactures fixtures, including companion board: MXKIT-Base, MXKIT-Core-3280

Version Update Record

Date	Version	Update Content
2019-08-08	1.0	Initial Document
2019-10-28	1.1	Update Wi-Fi Frequency parameter in abstract
2019-10-31	2.0	Update some package and photo information
2020-07-17	2.1	Update pin definition table
2021-04-27	2.2	Add compliance information
2021-11-30	2.3	Update electrical parameter

Copyright Notice

Catalog

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1. Introduction

EMC328x series modules are mainly used in high performance modules of Wi-Fi/BLE gateway applications in the Internet of Things. It has a dual-core microcontroller with ultra-high integration, supports 2.4 GHz Wi-Fi and BLE 5.0 wireless communication technology, and contains large capacity Flash, RAM to meet the data transmission, storage and protocol of various Internet of Things gateway applications. The need for conversion.

The module's built-in dual-core processor consists of a high-performance core and a high energy efficiency core. The core of high performance is a 32-bit core with a main frequency up to 200 MHz. Based on the latest ARM v8-M architecture, it not only has low power consumption, but also can complete floating-point operation and DSP instruction processing, thus efficiently completing the processing of IOT gateway data. The energy efficient core frequency is 20MHz, which provides a simplified instruction system for ultra-low power applications, so that the system can keep standby for a long time.

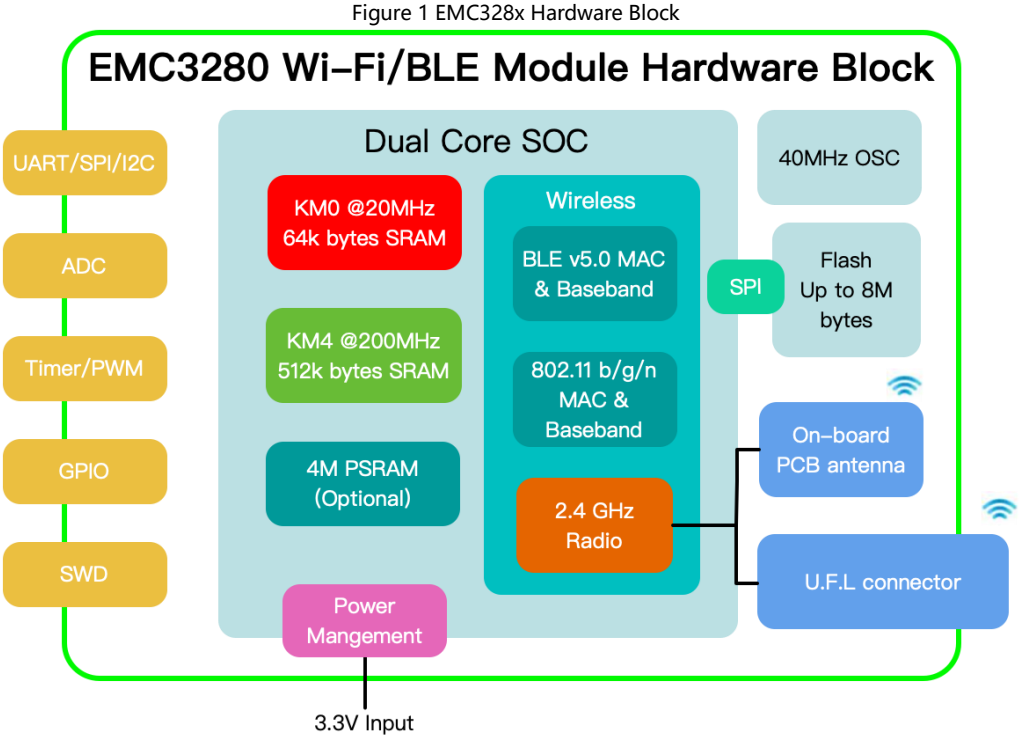
2.4 GHz Wi-Fi provides a cost-effective solution for stable access to the Internet. BLE 5.0 technology can not only facilitate users to complete the rapid configuration of products, but also realize the intelligent networking of a large number of devices through Mesh technology.

Large-capacity Flash and RAM space allows developers to build large-capacity Mesh network to implement complex Internet of Things cloud service communication protocol, gateway protocol. Local processing of data at the edge of the Internet of Things brings higher real-time and intelligent application logic for Internet of Things applications. Rich peripheral interfaces can maximize system customization and expansion, and facilitate the construction of innovative application products.

Shanghai MXCHIP provides MXOS software platform to support module development, providing efficient development environment, perfect communication protocol stack, rich sample programs and typical applications. At the same time, EMC328x series modules are also the hardware platform certified by AliOS. The following diagram is the hardware block diagram of EMC328x module, which mainly includes:

- ARM Dual Core Wireless Microcontroller
- PCB antenna or external antenna pedestal
- Power supply and communication interface
- Flash memory

Figure 1 EMC328x Hardware Block



1.1. Peripheral List

Item	Peripherals	Comment	Note
UART	HS_UART1	Internal connection to Bluetooth	1
	HS_USI_UART		1
	LP_UART1	Low power mode wake up	1
	LP_UART0	Log UART，Low power mode wake up	1
SPI	HS_SPI1	Supports main mode, clock up to 25MHz	1
	HS_USI_SPI	Support master / slave mode, clock up to 25MHz	1
RTC	RTC_OUT		1
	EXT_32K		1
IR	IR		1
I²C	LP_I2C	Standard mode (up to 100Kbps) Fast mode (up to 400Kbps)	1
	HS_USI_I2C	Standard / fast / high speed mode (up to 3.33Mbps)	1
HS_PWM	HS_PWM0 ~ 17		8
LP_PWM	LP_PWM0 ~ 5	Support low power mode	4
DMIC	DMIC		1
SGPIO	SGPIO		1
Key-Scan	Key-Scan		4x2/3x3
Wake Pin	Wake Pin	Wake up from deep sleep mode	6
HS_TIM4_TRIG	HS_TIM4_TRIG	Timer capture pin	1
HS_TIM5_TRIG	HS_TIM5_TRIG	Timer capture pin	1
Analog Pin	USB	USB master-slave mode, the main mode supports mass storage class	1
	ADC	0 ~ 3.3V	3

2. Characteristic

2.1. System and storage

- **Processor**
  - Dual Core Processor
  - KM4: Adopt ARM's latest v8M architecture, compatible with Cortex-M4F instruction set
  - KM4: Adopt ARM's latest v8M architecture, compatible with Cortex-M0 instruction set
  - Two cores have equal access to SRAM, peripherals and registers
  - Internal communication between two processors
- **KM4 Processor**
  - Compatible with Cortex-M4F instruction set, supporting FPU, DSP, MPU and TrustZone-M technology
  - Operating frequency up to 200MHz (configurable)
  - SWD serial debugging interface, support 8 hardware breakpoints and 4 observation points (SWO interface function is not supported)
  - Built-in NVIC interrupt vector table
  - System timer System tick timer.
  - 32KB I-Cache and 4KB D-Cache.
- **KM0 Processor**
  - Compatible with Cortex-M0 instruction set
  - Operating frequency up to 20MHz
  - Built-in NVIC interrupt vector table
  - SWD serial debugging interface, supporting 4 hardware breakpoints and 2 observation points (SWO interface function is not supported)
  - System timer System tick timer.
  - 32KB I-Cache and 4KB D-Cache
- **KM4 CPU On-Chip memory**
  - Up to 512KB of continuous space main SRAM with a frequency of 200MHz
  - (Specific models) can choose up to 4MB PSRAM, frequency up to 50MHz50MHz, 8bit DDR (specific models)
- **KM4 CPU On-Chip memory**
  - Up to 64KB continuous space main SRAM with a frequency of 64MHz
  - Reserve 1KB SRAM for saving data in low power mode
- **GDMA**
  - KM4 and KM0 both contain a GDMA controller.

- HS-GDMA0 Support 6 channels and support TrustZone-M technology
- LP -GDMA0 supports 6 channels

- **Flash**
  - SPI Flash controller with Cache
  - Support ICP technology and program Flash directly
- **General-Purpose I/O (GPIO)**
  - 16 GPIOs with upper and lower pull-down resistors
  - Configurable external interrupt triggered by rising edge, falling edge and double edge

2.2. Wireless Communication

- **Wi-Fi**
  - 802.11 b/g/n 1x1, 2.4GHz
  - Support 20MHz/40MHz bandwidth, 802.11n rate reaches MCS7
  - Low-power architecture, low-power transceiver for short-range applications, low-power beacon listening mode, low-power RX mode, low-power suspend mode (DLPS)
  - Support external amplifier
- **BT BLE**
  - Support low-power Bluetooth
  - Support both master and slave modes
  - High power mode (10dBm, sharing PA with Wi-Fi)
  - Built-in Wi-Fi/Bluetooth single antenna coexistence mechanism

2.3. Safety

- AES/DES/SHA hardware encryption algorithm engine
- Support TrustZone-M technology
- Secure boot secure boot
- SWD debug interface protection to prevent the debug interface from accessing protected and forbidden areas
- Support RSIP, automatic decryption of Flash data

2.4. Communication interface

- **USB**
  - Support USB 2.0, high speed / full speed / low speed mode
  - Support DMA transfer, 1.5Kbyte input block buffer, 1.5Kbyte output block buffer

- **SPI**
  - Support Motorola SPI serial data transmission
  - Support master-slave mode
  - Provide 1 SPI interface
  - SPI1 (Normal speed): Configurable in master mode with clocks up to 25MHz
  - Support DMA transmission
  - Configurable independent interrupt
  - FIFO Depth: Receive and transmit FIFO queues with 64 words depth, 16 bits per word.
  - Hardware/software slave device selection function: You can use special hardware to select the pin from the device chip or use software to control the GPIO mode as the chip select signal of the SPI slave device.

  Programmable features:
  - Clock frequency: Dynamically control the bit rate of data transmission when set to master mode
  - The size of each transmitted data (4 to 16 bits)
  - Clock polarity and phase
  - When setting to receive serial data in master mode, you can set the delay time of sampling to achieve higher serial bit rate.
- **UART**
  - Supported UART formats: 1 start bit, 7/8 data bits, 0/1 parity bits and 1/2 stop bits
  - Support hardware flow control
  - Support for interrupt control
  - Support IrDA
  - Support loopback mode for testing
  - Support TX, RX uses different clocks
  - Tx channel can use the baud rate generator with fractional number to generate accurate clock
  - Rx channel supports low power mode
  - Monitor and eliminate baud rate error and drift on the Rx channel
  - Support DMA transmission
- **IR (Infra Ray)**
  - Support carrier frequency range: 25KHz ~ 500KHz, duty cycle: 1/2 ~ 1/5
  - Support infrared diode input, support infrared receiver module input
  - 32*4 bytes Tx FIFO, 32*4 bytes Rx FIFO
- **One wire (SGPIO)**
  - Single-wire communication interface for secure encryption chip

- **I2C**
  - Two-wire I2C serial interface consisting of data line (SDA) and clock line (SCL)
  - Supports one I2C interface, supports two standard modes with a maximum rate of 100Kbps and a high-speed mode of 400Kbps, and supports clock stretching.
  - Support I2C master or slave device
  - Support 7-bit or 10-bit address addressing and support mixed transmission
  - Receive and send buffers with 16 words depth
  - Support DMA for data transmission and reception
  - Support bus arbitration mechanism to realize communication capability of multi-master devices
  - Wake-up from device address match for low power consumption
  - Software configurable parameters: SDA hold time, slave address, etc.
  - Programmable SDA and SCL signal digital filters for filtering noise on signal lines

2.5. Timer

- **Basic Timer（HS_TIM0 ~ HS_TIM3，LP_TIM0 ~ LP_TIM3)**
  - Clock source: 32KHz, accuracy: 32 bits, counting mode: counting up
  - Support interrupt trigger, sleep mode wake-up
- **PWM Timer（HS_TIM5 ，LP_TIM5)**
  - Channel: HS_TIM5 x 8 , LP_TIM5 x 4
  - Clock source: XTAL, accuracy: 16 bits, counting mode: increment counting, frequency division: 8 bits
  - 1 x input capture pin
  - LP_TIM5 can work in low power mode
- **Real Time Clock (RTC)**
  - Independent BCD counter
  - Day/hour/minute/second, 12 or 24 hour format clock
  - Software programmable clock compensation
  - An alarm that can be triggered by any combination of time domains and generate an interrupt
  - Digital calibration circuit
  - Register write protection

2.6. Human-Computer Interaction Interface

- **Matrix keyboard**
  - 6 IO ports, up to 4 x 2, 3 x 3 matrix keyboard scanning
  - Number of configurable keyboard rows and columns
  - Configurable scan clock, scan interval and release time

- Support interrupt trigger
- Provide 12-bit 16-depth FIFO for saving keyboard press and release events
- Support low power loss, button time can wake up the CPU from low power mode

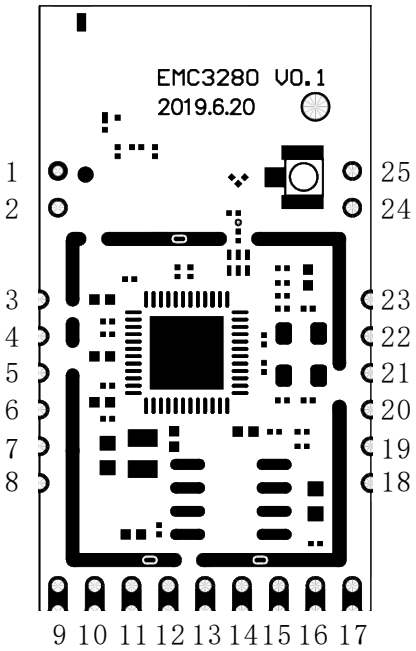
2.7. Analog processing

- **ADC And Voltage Comparator**
  - Accurate 12-bit successive approximation register ADC converter
  - Number of channels
  - 3 external 3.3V channels
  - 3 internal channels
  - Configurable inputs: single-ended mode and differential mode
  - Support DMA transmission
  - Sampling trigger source: software, timer
  - A low-power voltage comparator for measuring battery power
  - Triggerable wake-up circuit

3. Pin Definition

3.1. Pin Arrangement

Figure 2 EMC3280 Pin Arrangement



3.2. Pin Definition

3.2.1. Definition of General Pin

Table 1 Pin Definition

Pin Number	Name (function after reset)	Default State [2]	Function 1 (UART DATA)	Function 2 (LOG UART RTS/CTS)	Function 3 (SPI)	Function 5 (IR)	Function 7 (I2C)	Function 9 (HS PWM)	Function 10 (LP PWM)	Function 14 (USB)	Function 16 (SGPIO)	Function 22 (HS timer trig)	ADC Channel
1,3	PB3 (SWCLK)	High-Z											ADC6
2,4	PA27[1] (SWDIO)	Internal UP		LP_UART_RTS									
5	PB2	High-Z	LP_UART_RXD								SGPIO	HS_TIM5_TRIG	ADC5
6	PB1	EfusePullCtrl4	LP_UART_TXD								SGPIO_OUT	HS_TIM4_TRIG	ADC4
7	PB20	High-Z	HS_USI_UART_TXD				HS_USI_I2C_SCL	HS_PWM12	LP_PWM0				
8	PB21	High-Z	HS_USI_UART_RXD				HS_USI_I2C_SDA	HS_PWM13	LP_PWM1				
9	PA26	High-Z	LP_UART_TXD		HS_USI_SPI_MISO	IR_RX	LP_I2C_SDA	HS_PWM5	LP_PWM5	HSDP			
10	PA25	EfusePullCtrl2	LP_UART_RXD		HS_USI_SPI_MOSI	IR_TX	LP_I2C_SCL	HS_PWM4	LP_PWM4	HSDM			
11	nRESET		nRESET										
12	PA30[1]	External UP			HS_USI_SPI_CLK			HS_PWM7	LP_PWM1	VBUS_OTG			
13	PA28	EfusePullCtrl3		LP_UART_CTS	HS_USI_SPI_CS			HS_PWM6	LP_PWM0	RREF			
14	PA12[1]	High-Z	LP_UART_TXD		SPI1_MOSI			HS_PWM0	LP_PWM0				
15	PA13[1]	EfusePullCtrl0	LP_UART_RXD		SPI1_MISO			HS_PWM1	LP_PWM1				
16	VDD		VDD										
17	VSS		VSS										
18	NC												
19	PA14[1]	High-Z		LP_UART_RTS	SPI1_CLK								
20	NC												
21,24	PA7[1] (UART_LOG_TXD)	Internal UP		UART_LOG_TXD									
22,25	PA8 (UART_LOG_RXD)	Internal UP		UART_LOG_RXD									
23	PA15[1]	EfusePullCtrl1		LP_UART_CTS	SPI1_CS								

(1). Special function capture pin, the module will detect the status of these pins when starting up and enter special functions, please refer to chapter 3.2.3

(2). The default state of the pin. When the Reset button is pressed, all GPIO ports will remain in their previous state. When the Reset button is released, the GPIO state returns to the state described in "Default State" in Table 1, where EfusePullCtrlx indicates that the default state of the pin is the status bits in eFuse are determined.

(3). The time from system power-up to GPIO power supply can be divided into three phases:

- The supply voltage rises to 1.5V and the internal AON_LDO voltage rises to 0.5V. Determined by 3.3V/1.8V power-on time
- The internal analog circuit of the chip needs 6ms to supply power to the Reset button, and then the digital circuit starts to work.
- After 300us~1.5ms, the general GPIO is powered, the default level will take effect.
- Phase 2 and Phase 3 require a total of 6.3ms ~ 7.5ms

3.2.2. Low Power Pin Definition

Low-power pins can wake the module from the Deep Sleep state and are located on the keyboard scan function pin.

Table 2 Low Power Pin Definition

Pin Number		Name (function after reset)	Function 28 (Ext32K)	Function 29 (key scan row)	Function 30 (key scan col)	Function 31 (wakeup)	PX_FUNC_DEFAULT
EMC3280	EMC3285						
14	9	PA12		KEY_ROW0		LGPIO0	GPIOC_LP0
15	8	PA13		KEY_ROW1		LGPIO1	GPIOC_LP1
19	6	PA14	RTC_OUT	KEY_ROW2		LGPIO2	GPIOC_LP2
23	7	PA15	RTC EXT_32K	KEY_ROW3	KEY_COL6	LGPIO3	GPIOC_LP3
10	11	PA25			KEY_COL1	LGPIO2	GPIOC_LP10
9	12	PA26			KEY_COL0	LGPIO3	GPIOC_LP11

3.2.3. Special Function Capture Pins

The status of these pins is detected during power-up of the module, allowing access to certain special modes and functions. These features are hardware determined and cannot be modified.

Table 3 Special function capture pin

Pin Name	Trap Function	State	Description
PA7	UART_DOWNLOAD	High (Default)	Normal boot application
		Low	Boot ROM code and enter flash download mode
PA12	ICFG0	Test mode, if not entering test mode, can be ignored	
PA13	ICFG1	Test mode, if not entering test mode, can be ignored	
PA14	ICFG2	Test mode, if not entering test mode, can be ignored	

PA15	ICFG3	Test mode, if not entering test mode, can be ignored	
PA27	NORMAL_MODE_SEL	High (Default)	Normal boot application
		Low	Enter test mode, use PA12 ~ PA15
PA30	SPS_SEL	High (Default)	SWR mode (10K pull-up inside the module)
		Low	LDO mode

If the module firmware is developed using the MXOS development platform provided by MXCHIP, the application will also check the status of the following pins during the boot process to enter a special working mode. These features can be adjusted by modifying the code. The default features are described below. Before the final production, if these functions are useful, a verification test is required.

There are currently three working modes to choose from:

- Normal: The application runs normally.
- ATE: Runs the RF test mode, in which the RF transmit power, receive sensitivity, and RF parameters can be tested. Interact with the ATE command using UART_LOG (TX: PA7, RX: PA8).
- QC: Run the factory test mode, output QC information through LP_UART (TX: PB1, RX: PB2), and cooperate with the detection program running on the PC, which can be used to verify the firmware version in the module, login information of the cloud service and basic hardware. Features.

When detecting the pin state, the firmware first sets the mode of PB1 and PB23 to the input pull-up. Therefore, if the external does not interfere, the IO state is high, and the default working state is: Normal.

Table 4 Firmware special function capture pin

Firmware Working Mode	PA14 (BOOT)	PA15 (STATUS)
Normal	1	No Detection
ATE	0	1
QC	0	0

4. System memory space

The EMC328x module contains the following memory units::

4.1. KM4 Embedded SRAM

The KM4 core contains up to 512K bytes of continuous on-chip SRAM memory. The embedded SRAM can pass byte (8 bits), halfword (16 bits) or single word (32 bits). It is divided into two blocks, which are accessible by the KM4 and KM0 cores.

- KM4 SRAM1 (up to 256KB)
- KM4 SRAM2 (up to 256KB)

Dividing the SRAM into two delivery device ports allows the user's application to achieve better performance. For example, SRAM can be accessed by both the CPU and the DMA controller without causing delays. Generally speaking, when the DMA is reading and writing data from the peripheral to the SRAM, the CPU also accesses the SRAM to read and write data of other peripherals. Therefore, the read and write of different peripheral data are placed in different SRAM blocks. Can reduce the delay. In addition, the SRAM is read and written alternately to access the same peripheral data sequence. For example, the CPU is notified when the DMA is reading and writing to the RAM buffer and is ready to operate on the next buffer. In this way, the CPU and DMA can simultaneously operate different buffers in different SRAM blocks, reducing the delay of access.

In the power supply area, the entire SRAM is also divided into 3 blocks:

- SRAM_PD1 (up to 256KB)
- SRAM_PD2 (up to 128KB)
- SRAM_PD3 (up to 128KB)

Each block can be individually set to open in the Power Management Unit (PMU), and this SRAM can be recovered as quickly as the system wakes up from sleep mode.

4.2. KM0 Embedded SRAM

The KM0 core contains up to 64K bytes of memory. The embedded SRAM can pass byte (8 bits), halfword (16 bits) or single word (32 bits). Can be accessed by the KM4 and KM0 cores.

4.3. KM4 Extension SRAM

f you don't use Bluetooth, the KM4 core can scale an extra 64KB of SRAM. The SRAM can also be accessed by KM4 and KM0 at speeds up to 50MHz*32 bits.

4.4. Retention SRAM

The chip also provides 1KB of SRAM for saving data in the deep sleep mode with the lowest power consumption. This SRAM can also be accessed by KM4 and KM0.

4.5. SPI Flash Memory

The CPU manages access to the flash memory from the I-Code and D-Code buses via the built-in SPI Flash Control Unit (SPIC). At the same time, operations such as erasing, programming, and read-write protection are implemented, and instruction prefetching and caching are used to accelerate the execution of stored code on the flash memory.

4.6. PSRAM

Optional 4M byte PSRAM with 50MHz DDR memory.

4.7. System Storage Control Address Assignment

The address allocation is shown in Table 5:

Table 5 System Storage Space

Base Address	Top Address	Size	Function	Description
0x0000_0000	0x0001_FFFF	128KB	KM0 ITCM ROM (actually 96KB)	32MB: KM0 Memory Address
0x0002_0000	0x0002_7FFF	32KB	KM0 DTCM ROM (actually 16KB)	
0x0002_8000	0x0007_FFFF	352KB	RSVD	
0x0008_0000	0x0008_FFFF	64KB	KM0 SRAM	
0x0009_0000	0x000B_FFFF	192KB	RSVD	
0x000C_0000	0x000C_3FFF	16KB	Retention SRAM (1KB) (the same port with KM0 SRAM)	
0x000C_4000	0x000F_FFFF	240KB	RSVD	
0x0010_0000	0x01FF_FFFF	31MB	RSVD	
0x0200_0000	0x07FF_FFFF	96MB	External PSRAM	224MB: External Memory Address
0x0800_0000	0x0FFF_FFFF	128MB	External FLASH	
0x1000_0000	0x1007_FFFF	512KB	KM4 SRAM	256MB: KM4 Memory Address
0x1008_0000	0x100D_FFFF	384KB	RSVD	
0x100E_0000	0x100E_FFFF	64KB	Extension SRAM0 from Bluetooth	
0x100F_0000	0x100F_FFFF	64KB	Extension SRAM1 from Wi-Fi	
0x1010_0000	0x1013_FFFF	256KB	KM4 ITCM ROM	
0x101C_0000	0x101D_7FFF	96KB	KM4 DTCM ROM	
0x101E_0000	0x101F_FFFF	256KB	RSVD	
0x1020_0000	0x1FFF_FFFF	254MB	RSVD	
0x2000_0000	0x3FFF_FFFF	512MB	RSVD	Reserved
0x4000_0000	0x47FF_FFFF	128MB	KM4 Peripherals	128MB: KM4 Peripherals Address
0x4800_0000	0x4FFF_FFFF	128MB	KM0 Peripherals	128MB: KM0 Peripherals Address
0x5000_0000	0x57FF_FFFF	128MB	KM4 Peripherals Secure	128MB: KM4 Peripherals Secure Address
0x5800_0000	0xFFFF_FFFF	2816MB	RSVD	Reserved

When developing firmware using the MXOS platform provided by MXCHIP, 4MB of Flash space is pre-allocated as follows:

Table 6 Flash Storage space partition

Name	Description	Start Address	Size
KM0 Boot	KM0 kernel bootloader	0x0800_0000	20 Kbytes
Backup	System data backup area	0x0800_2000	4 Kbytes
System Data	System data	0x0800_3000	4 Kbytes
KM4 Boot	KM4 kernel bootloader	0x0800_4000	8 Kbytes
APP1	Application partition 1, when the OTA is upgraded, switch boot with APP2.	0x0800_6000	1504 Kbytes
KV	Key/Value data storage area	0x0817_E000	16 Kbytes
BT FTL	Bluetooth binding information storage area	0x0818_2000	12 Kbytes
APP2	Application partition 2, when the OTA is upgraded, the boot is switched with APP1.	0x0818_8000	1504 Kbytes
USER	User use partition	0x0830_0000	1024 Kbytes

5. Electrical parameters

5.1. Absolute maximum parameters

Operation of the module outside of its absolute maximum ratings may result in permanent damage. At the same time, long-term exposure to the maximum rated conditions will affect the reliability of the module.

Table 7 Absolute Maximum Parameter: Voltage

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	Voltage	–0.3	3.6	V
V_{IN}	Input voltage on any other pin	V_{SS}–0.3	V_{DD}+0.3	V

5.2. Operating voltage and current

Table 8 Operation parameter: voltage and current

Symbol	Note	Specification			
		Min.	Typical	Max.	Unit
V_{DD}	Voltage	3.0	3.3	3.6	V
I_{VDD}	3.3V Rating Current (with internal regulator and integrated CMOS PA)			450	mA

Table 9 Average power consumption under 3.3V

Operation Mode		Conditions	Average Current	Unit
Power Mode	Scenario			
Deepsleep	Deepsleep	RTC timer 1KB retention RAM	7~8	μA
	Deepsleep with Key-Scan	RTC timer 1KB retention RAM Key-Scan	12~13	μA
	Deepsleep with Cap-Touch (average current)	RTC timer 1KB retention RAM Cap-Touch	20	μA
Sleep	WoWLAN sleep power	KM4 power gate KM0 clock gate All RAM retained Wi-Fi retained	30~50	μA
Active	Wi-Fi Rx Idle	HT20 MCS0~7 normal mode KM4 in active mode Rx idle	81	mA
		HT20 MCS0~7 ultra-low power mode KM4 in active mode Rx idle	60	mA

Operation Mode		Conditions	Average Current	Unit
Power Mode	Scenario			
	Wi-Fi Rx UDP	HT20 MCS0~7 ultra-low power mode KM4 in active mode UDP Rx @ 8Mbps	67	mA
WoWLAN	WoWLAN Rx Beacon	Rx beacon mode @ normal mode KM4 in sleep mode	45	mA
		Rx beacon mode @ ultra-low power mode KM4 in sleep mode	39	mA
	WoWLAN DTIM=1 (Average)	KM4 in sleep mode All SRAM retained Wi-Fi retained Open space	1.1~2	mA

Table 10 RF consumption under 3.3V, 2442MHz

Operation Mode	Current	Unit
1T-MCS7/BW40M (15dBm)	206	mA
1T-MCS7/BW20M (15dBm)	204	
1T-Legacy_OFDM54M (16dBm)	214	
1T_CCK11M (18dBm)	257	
1R-Idle/BW40	52	
1R-MCS7/BW40M (Pin= -60dBm)	61	
1R-MCS7/BW20M (Pin= -60dBm)	62	
1R-Legacy_OFDM54M (Pin= -60dBm)	61	
1R-CCK11M (Pin= -60dBm)	52	
RF Standby	24	
RF Disable	24	

5.3. Digital IO DC Characteristics

The electrical characteristics of the module digital IO port are divided into two cases: 1.8V power supply and 3.3V power supply, which are described in Table 10 and Table 11, respectively.

Table 11 Operating Parameters: Digital IO DC Characteristics (3.3V)

Symbol	Note	Conditions	Specification			
			Min.	Typical	Max.	Unit
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	9.58	9.59	13.43	V
V_{OL}	Output-Low Voltage	LVTTL			0.4	V
I_{IL}	Input-Leakage Current	V_{IN} = 3.3V/0V	-10	±1	10	μA

5.4. Temperature

Table 12 Storage Temperature and Operating Temperature

Symbol	Ratings	Max	Unit
T_{STG}	Storage temperature	–55 to +125	℃
T_A	Working temperature	-20 to +85	℃

5.5. RF Parameters

Table 13 RF Parameters

Item	Specification
Operating Frequency	2.412~2.484GHz
Channel BW	20MHz，40MHz
Antenna Interface	1T1R, single-stream
Wi-Fi Standard	IEEE 802.11b/g/n
Modulation Type	11b: DBPSK, DQPSK, CCK for DSSS 11g: BPSK, QPSK, 16QAM, 64QAM for OFDM 11n: MCS0~7, OFDM
Data Rates	11b: 1, 2, 5.5 and 11Mbps 11g: 6, 9, 12, 18, 24, 36, 48 and 54 Mbps 11n: MCS0~7, up to 150Mbps
Antenna type	One U.F.L connector for external antenna PCB printed ANT (Reserve)

Note: The following Tx test data is typically recorded in a normal temperature environment with Tx lasting about 20 seconds.

5.5.1. Wi-Fi RF characteristic

IEEE 802.11b mode

Table 14 IEEE 802.11b mode TX/RX characteristic

Item	Description			
Mode	IEEE802.11b			
Channel	CH1 to CH13			
Data Rates	1, 2, 5.5, 11Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				
11b Target Power@1Mbps	15.0	16.5	18.0	dBm
11b Target Power@11Mbps	15.0	16.5	18.0	dBm
Spectrum Mask @ target power				
fc +/-11MHz to +/-22MHz	-	-	-30	dB
fc > +/-22MHz	-	-	-50	dB

Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
1~11Mbps	-	-	35% (or -11dB)	
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
1Mbps (FER≦8%)	-	-98	-	dBm
11Mbps (FER≦8%)	-	-88	-	dBm

IEEE802.11g mode

Table 15 IEEE 802.11g mode TX/RX characteristic

Item	**Description**			
Mode	IEEE802.11g			
Channel	CH1 to CH13			
Data Rates	6, 9, 12, 18, 24, 36, 48, 54Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				
11g Target Power@6Mbps	13.5	15.0	16.5	dBm
11g Target Power@54Mbps	13.0	14.5	16	dBm
Spectrum Mask @ target power				
fc +/- 11MHz	-	-	-20	dB
fc +/- 20MHz	-	-	-28	dB
fc > +/-30MHz			-40	dB
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
6Mbps	-	-30	-5	dB
54Mbps	-	-30	-25	dB
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
6Mbps (FER≦10%)	-	-93	-	dBm
54Mbps (FER≦10%)	-	-76	-	dBm

IEEE802.11n-HT20 mode

Table 16 IEEE 802.11n-HT20 mode TX/RX characteristic

Item	**Description**			
Mode	IEEE802.11n HT20			
Channel	CH1 to CH13			
Data Rates	MCS0/1/2/3/4/5/6/7, up to 65Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				

11n Target Power@MCS0	13.5	14.5	16	dBm
11n Target Power@ MCS7	12.5	14	15.5	dBm
Spectrum Mask @ target power				
fc +/- 11MHz	-	-	-20	dB
fc +/- 20MHz	-	-	-28	dB
fc > +/-30MHz			-45	dB
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
MCS0	-	-30	-5	dB
MCS7	-	-31	-27	dB
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
MCS0 (FER≦10%)	-	-93	-93	dBm
MCS7 (FER≦10%)	-	-73.5	-73	dBm

IEEE802.11n-HT40 mode

Table 17 IEEE 802.11n-HT40 mode TX/RX characteristic

Item	**Description**			
Mode	IEEE802.11n HT40			
Channel	CH1 to CH13			
Data Rates	MCS0/1/2/3/4/5/6/7, up to 135Mbps			
TX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Transmitter Output Power				
11n Target Power@MCS0	13.5	14.5	16	dBm
11n Target Power@ MCS7	12.5	14	15.5	dBm
Spectrum Mask @ target power				
fc +/- 22MHz	-	-	-20	dB
fc +/- 40MHz	-	-	-28	dB
fc > +/-60MHz	-	-	-45	dB
Frequency Error	-10	-2	+10	ppm
Constellation Error (peak EVM) @target power				
MCS0	-	-30	-5	dB
MCS7	-	-32	-27	dB
RX Characteristics	**Min.**	**Typical.**	**Max.**	**Unit**
Minimum Input Level Sensitivity				
MCS0 (FER≦10%)	-	-90	-	dBm
MCS7 (FER≦10%)	-	-71.5	-	dBm

5.5.2. Bluetooth RF characteristic

Table 18 BLE5.0 TX/RX characteristic

Item	DataRate	Min	Typical	Max	Remark
POWER_AVERAGE	LE_1M	6	8	10dBm	
Frequency Drift Error	LE_1M	-50KHz	-5	50KHz	
Carrier frequency offset and drift at NOC:					
ΔFn max	LE_1M	-150KHz	6.1	150KHz	
|F0-Fn|	LE_1M		2.37	50KHz	
|F1-F0|	LE_1M		2.1	20KHz	
|Fn-Fn5|	LE_1M		0.89	20KHz	
Modulation characteristics:					
ΔF1avg	LE_1M	225KHz	249	275KHz	
ΔF2avg	LE_1M	185KHz	238	275KHz	
ΔF2avg/▵F1avg	LE_1M	0.8	0.96		
ΔF2max	LE_1M	185KHz	245		
In-Band Emissions					
OFFSET_-2	LE_1M		-44.3	-20dBm	
OFFSET_-3	LE_1M		-46.6	-30dBm	
OFFSET_-4	LE_1M		-46.5	-30dBm	
OFFSET_-5	LE_1M		-50.6	-30dBm	
OFFSET_2	LE_1M		-46.1	-20dBm	
OFFSET_3	LE_1M		-45.7	-30dBm	
OFFSET_4	LE_1M		-44.4	-30dBm	
OFFSET_5	LE_1M		-50.2	-30dBm	
RX Characteristics					
Minimum Sensitivity	LE_1M	-	-98dBm	-97dBm	PER ≤30.8%

6. Antenna Information

The EMC328x has two specifications, PCB antenna and external antenna. Please refer to the order code for ordering. The IPX antenna connector is not soldered to the module using the PCB antenna. Better RF performance can be achieved by connecting an external antenna through an IPX connector.

6.1. PCB Antenna Parameters and Use

6.1.1. On-board PCB Antenna Parameter

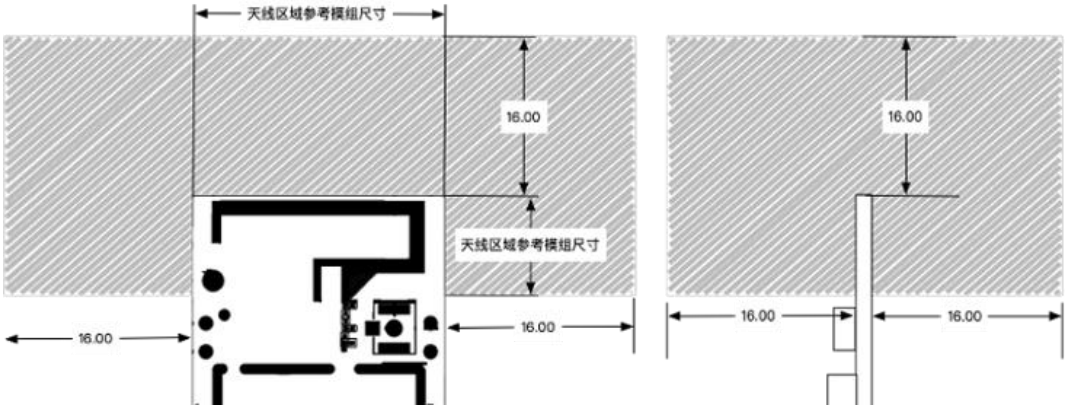
Table 19 On-board PCB Antenna Parameter of EMC3280

Item	Min.	Typical	Max.	Unit
Frequency	2400		2500	MHz
Impedance		50		Ω
VSWR			2	
Gain	-0.37dBi			
Efficiency	47%			

6.1.2. PCB Antenna use points

When using the PCB antenna on the module, you need to ensure that the distance between the motherboard PCB and other metal devices, connectors, PCB vias, traces, and copper is at least 16mm. The shaded areas in the figure below need to be kept away from metal components, sensors, sources of interference, and other materials that may cause signal interference.

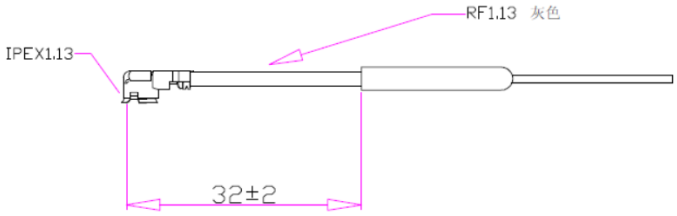
Figure 3 PCB Antenna minimum clearance area（unit：mm）



6.2. External antenna parameters and use

Users can select 2.4G antennas with different external dimensions and gains of no more than 2dBi depending on the application environment. The following is a copper tube antenna for an IPEX connector commonly used by MXCHIP.

Figure 4 Copper tube antenna size



Frequency Range：2400-2500 MHz

Input impedance: 50 OHM

Standing wave ratio: < 2.0

Gain: 2.0DBI

Polarization: vertical

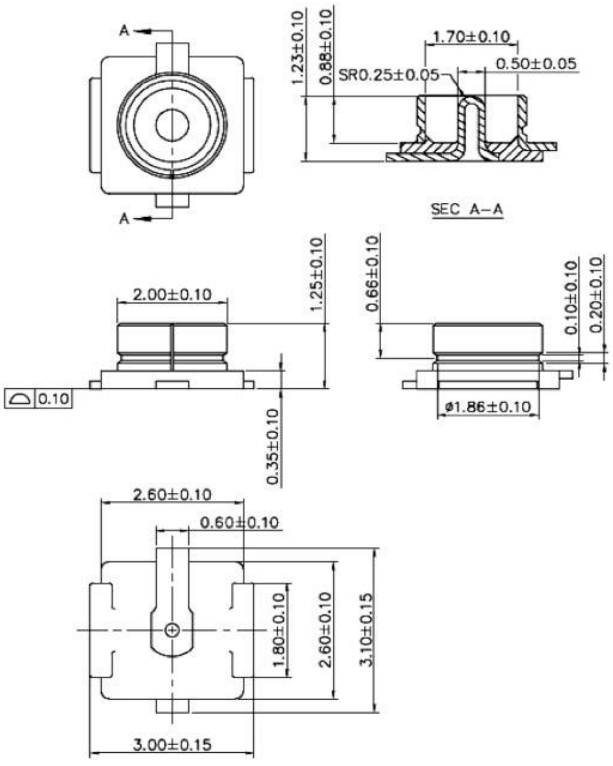
Directionality: Omnidirectional

Copper tube: 4.4*23mm

Wire: 1.13 gray line L-82mm

External antenna IPEX seat size:

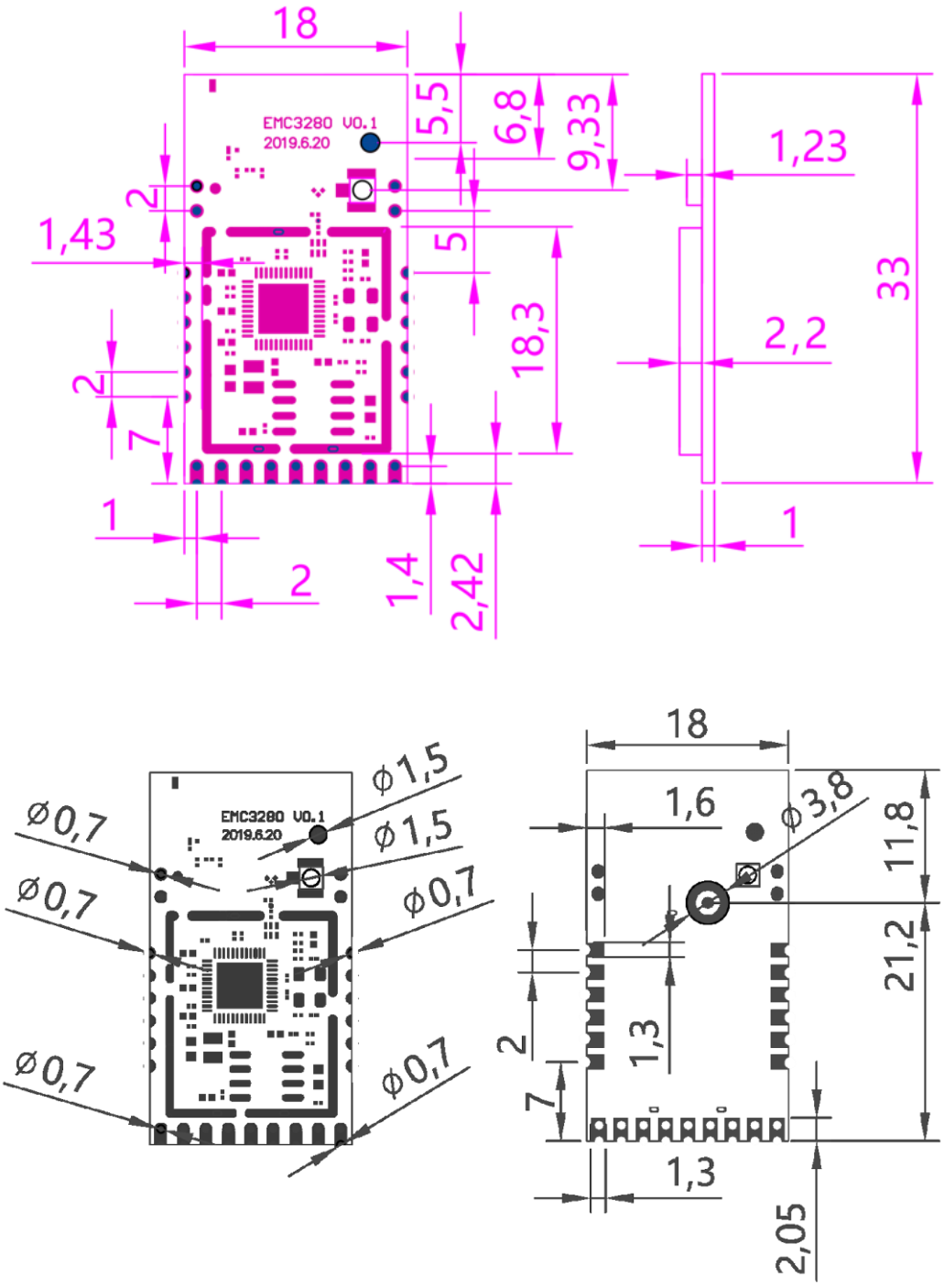
Figure 5 External antenna connector size chart



7. Assembly size and PCB package

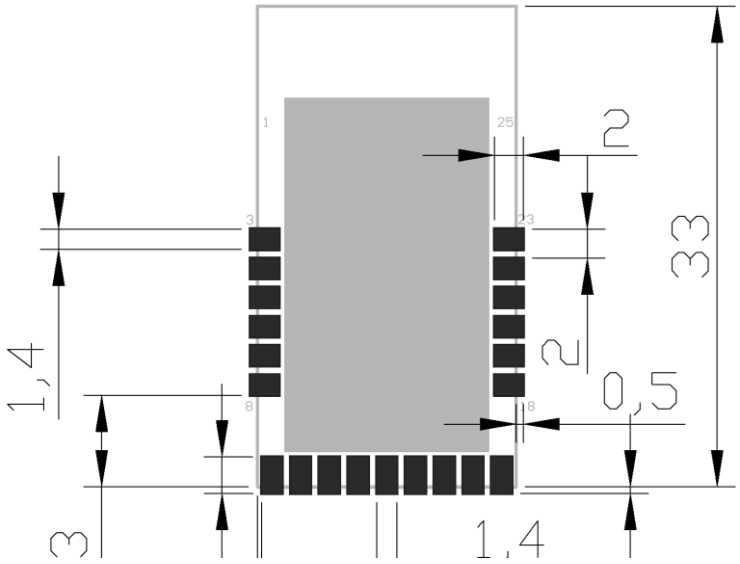
7.1. Final assembly size chart

Figure 6 EMC3280 three view（unit：mm, error：±0.1）



7.2. Recommended package drawing

Figure 7 EMC3280 PCB Package size（unit：mm）



8. Production Guidelines

MXCHIP stamp port packaging module must be SMT machine patches, module humidity sensitivity grade MSL3, after unpacking more than a fixed time patches to bake module.

- SMT patches require instruments
  - Reflow bonding machine
  - AOI detector
  - 6-8mm suction nozzle
- Baking requires equipment:
  - Cabinet oven
  - Anti-static, high temperature tray
  - Antistatic and heat resistant gloves

The storage conditions of MXCHIP module are as follows:

- Moisture-proof bags must be stored in an environment with temperature < 30 degree C and humidity < 85% RH.
- A humidity indicator card is installed in the sealed package.

Figure 8 Humidity Card

After the module is split, if the humidity card shows pink, it needs to be baked.

The baking parameters are as follows:

- The baking temperature is 120 5 and the baking time is 4 hours.
- The alarm temperature is set to 130 C.
- SMT patches can be made after cooling < 36 C under natural conditions.
- Drying times: 1 time.
- If there is no welding after baking for more than 12 hours, please bake again.

If the disassembly time exceeds 3 months, SMT process is forbidden to weld this batch of modules,

because PCB gold deposition process, over 3 months, pad oxidation is serious, SMT patch is likely to lead to virtual welding, leak welding, resulting in various problems, our company does not assume the corresponding responsibility.

Before SMT patch, ESD (Electrostatic Discharge, Electrostatic Release) protection should be applied to the module.

SMT patches should be made according to the reflow curve. The peak temperature is 250 C. The reflow temperature curve is shown in Chapter 10, Fig. 10.

In order to ensure the qualified rate of reflow soldering, 10% of the first patches should be taken for visual inspection and AOI testing to ensure the rationality of furnace temperature control, device adsorption mode and placement mode, and 5-10 patches per hour are recommended for visual inspection and AOI testing in subsequent batch production.

8.1. Precautions

- Operators at all stations in the entire production process must wear electrostatic gloves.
- Do not exceed the baking time when baking.
- It is strictly forbidden to add explosive, flammable or corrosive substances during baking.
- When baking, the module applies a high temperature tray to the oven to keep the air circulation between each module while avoiding direct contact between the module and the inner wall of the oven.
- When baking, please close the oven door to ensure that the oven is closed to prevent temperature leakage and affect the baking effect.
- Try not to open the door when the oven is running. If it must be opened, try to shorten the time for opening the door.
- After baking, the module should be naturally cooled to <36 °C before wearing the static gloves to avoid burns.
- When operating, strictly guard against water or dirt on the bottom of the module.
- The temperature and humidity control level of MXCHIP factory module is Level3, and the storage and baking conditions are based on IPC/JEDEC J-STD-020.

8.2. Secondary Reflow Profile

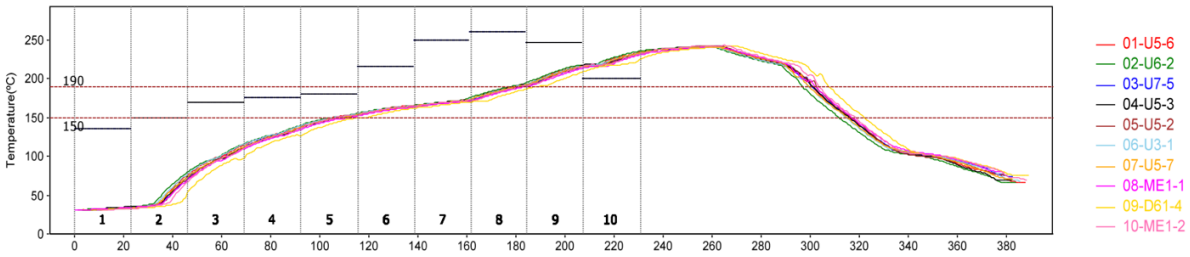
Solder paste type is recommended: SAC305, lead free. The number of reflows does not exceed 2 times. The peak temperature does not exceed 245 °C. The following is a typical furnace temperature profile setting.

Table 20 Typical furnace temperature setting

Welding furnace setting	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10

Upper temperature zone setting	135	150	170	175	180	215	250	260	247	200
Lower temperature zone setting	135	150	170	175	180	215	250	260	247	200

Figure 9 Typical secondary reflow profile



- Preheating temperature rise from 30 ° C to 150 ° C: 0-3 ° C / s, typical value: 1.2 ° C / s
- 150 ° C ~ 190 ° C immersion temperature: 60-100 seconds, typical value: 72 seconds
- Peak temperature: 245 ° C, typical value: 242 ° C
- Time above 220°C: 50 seconds to 90 seconds, typical value: 70 seconds
- 217 ° C cooling rate: -3 ~ 0 ° C / s, typical value: -2.0 ° C / s

8.3. Storage Condition

Figure 10 Storage Condition Diagram

9. Label Information

Figure 11 EMC3280 Product Label

1. Trademark of Shanghai MXCHIP Information Technology Co., Ltd.
2. CMIIT ID, SRRC No.
3. Module model
4. Module sub model
5. Wi-Fi MAC. Adding 1 to the MAC address of Wi-Fi is Bluetooth MAC.
6. Firmware version information
7. QR Code: the content is the MAC address of Wi-Fi

Appendix 1: Sales and Technical Support Information

If you need to consult or purchase this product, please call Shanghai MXCHIP Information Technology Co., Ltd. during office hours.

Office hours: Monday to Friday morning: 9:00 to 12:00, afternoon: 13:00 to 18:00

Contact Tel: +86-21-52655026

Address: 9th Floor, No. 5, Lane 2145, Jinshajiang Road, Putuo District, Shanghai

Zip code: 200333

Email: sales@mxchip.com